

FIG.1

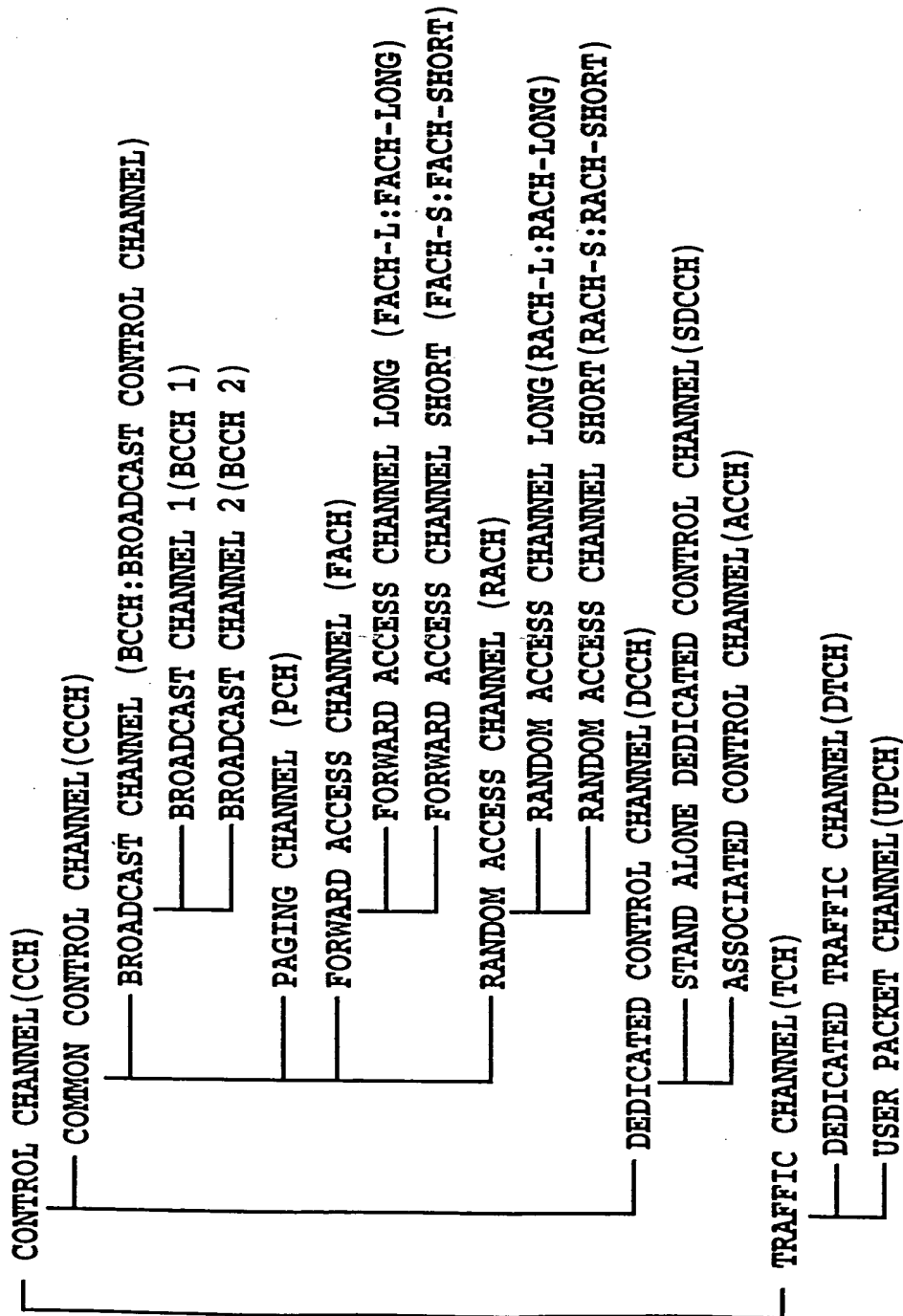


FIG.2

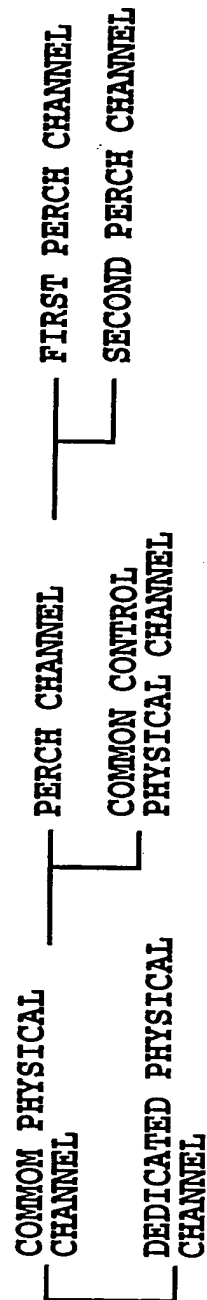


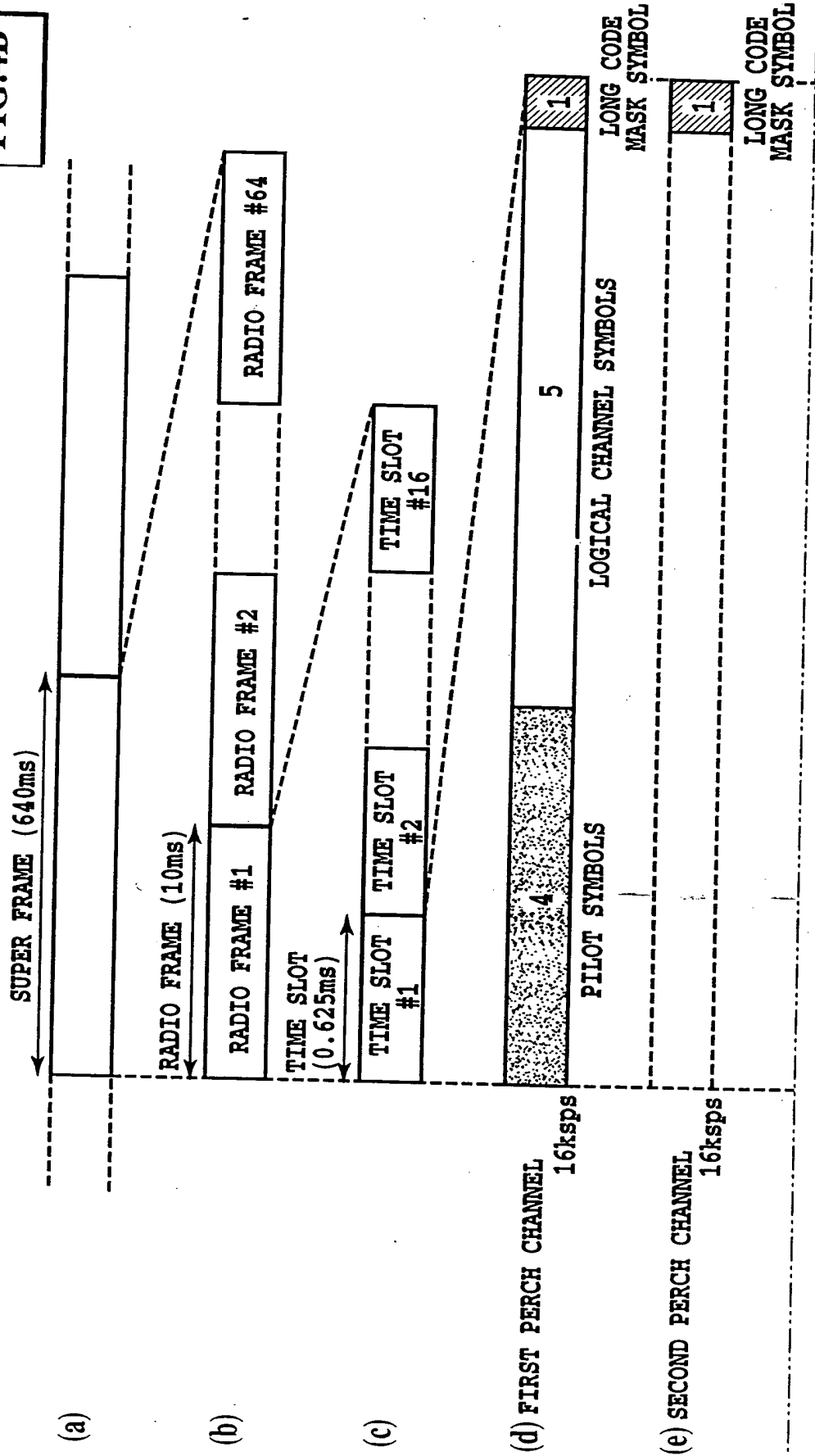
FIG.3

FIG.4

FIG.4A

FIG.4B

FIG.4A



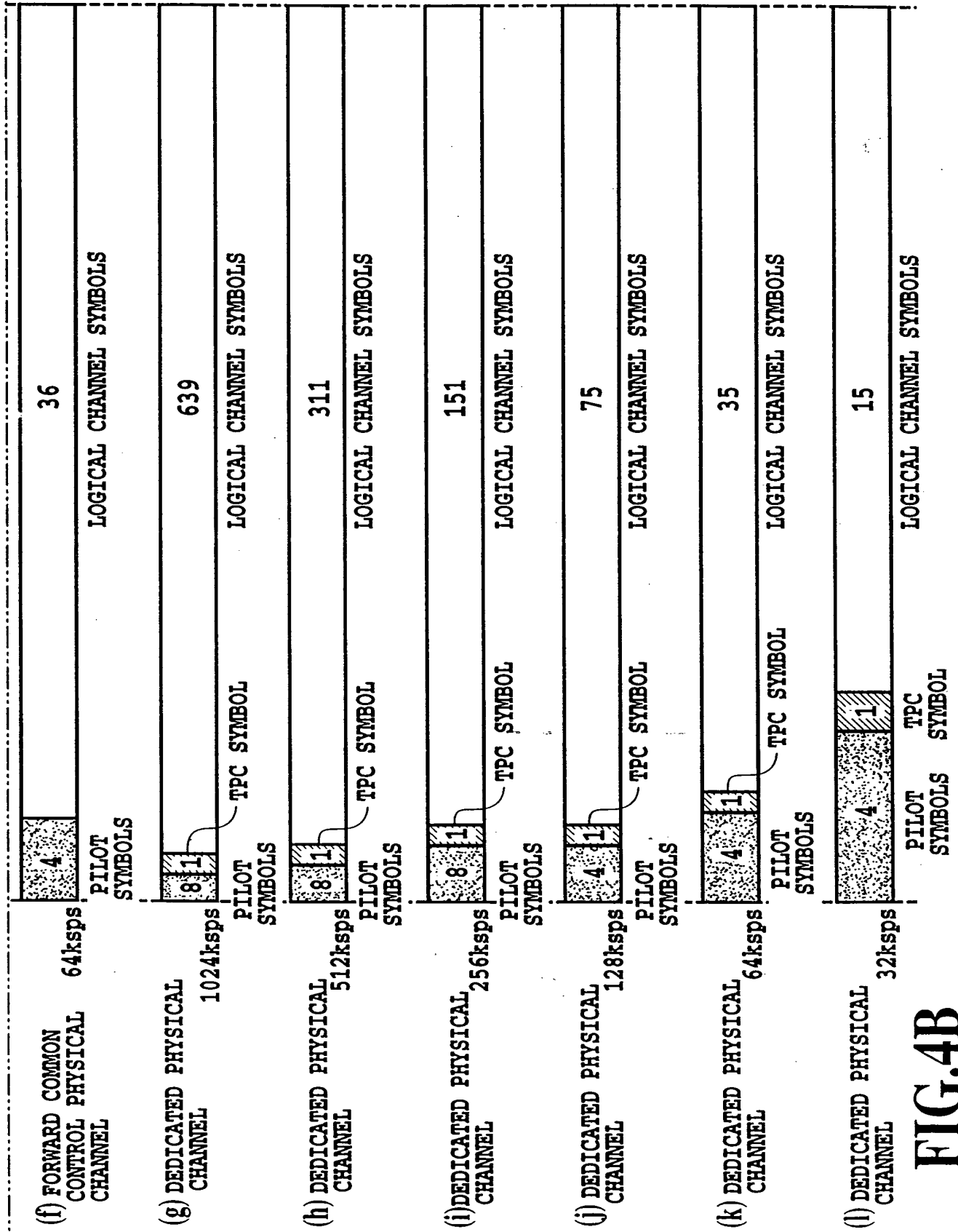


FIG.4B

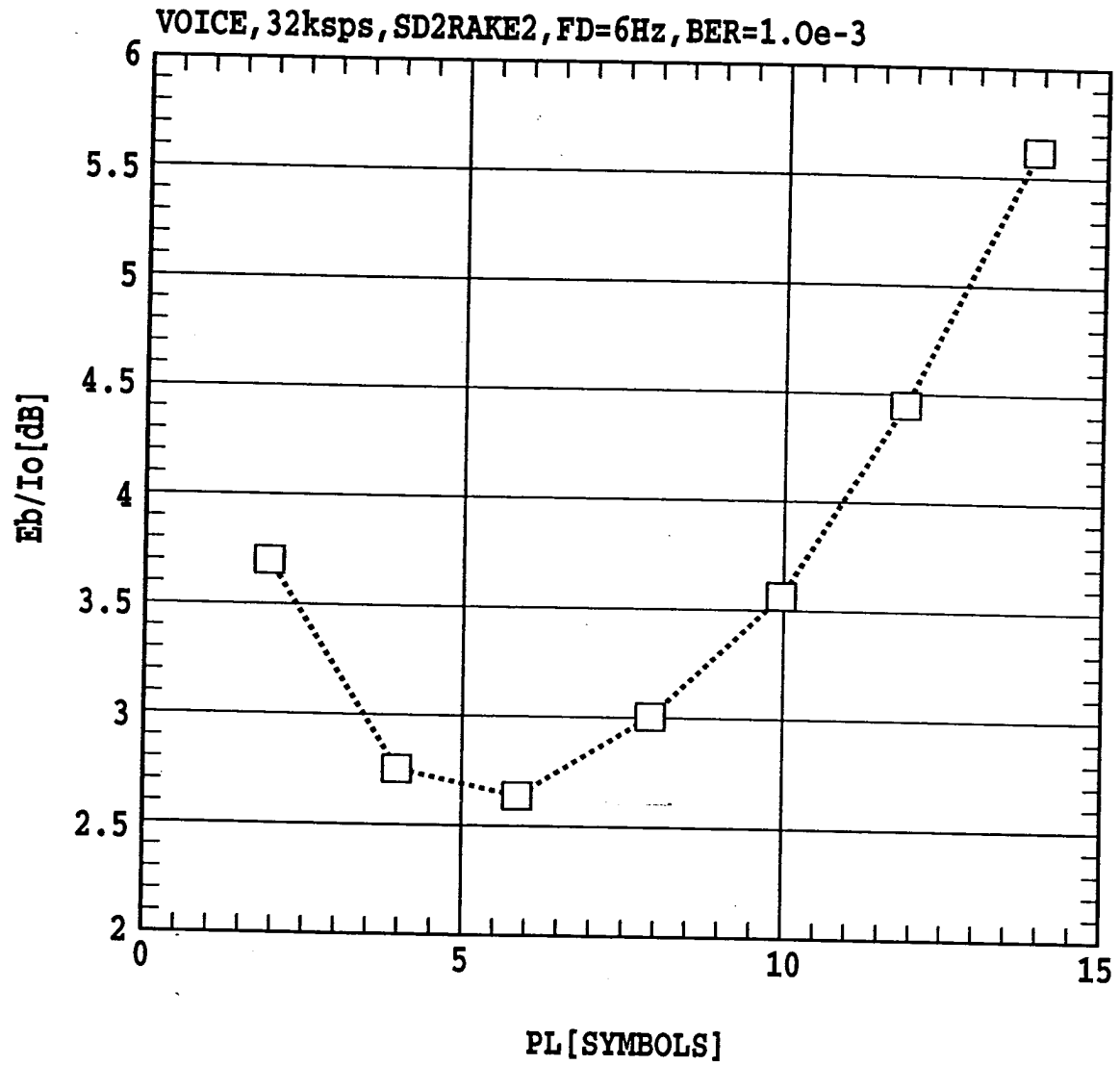


FIG.5

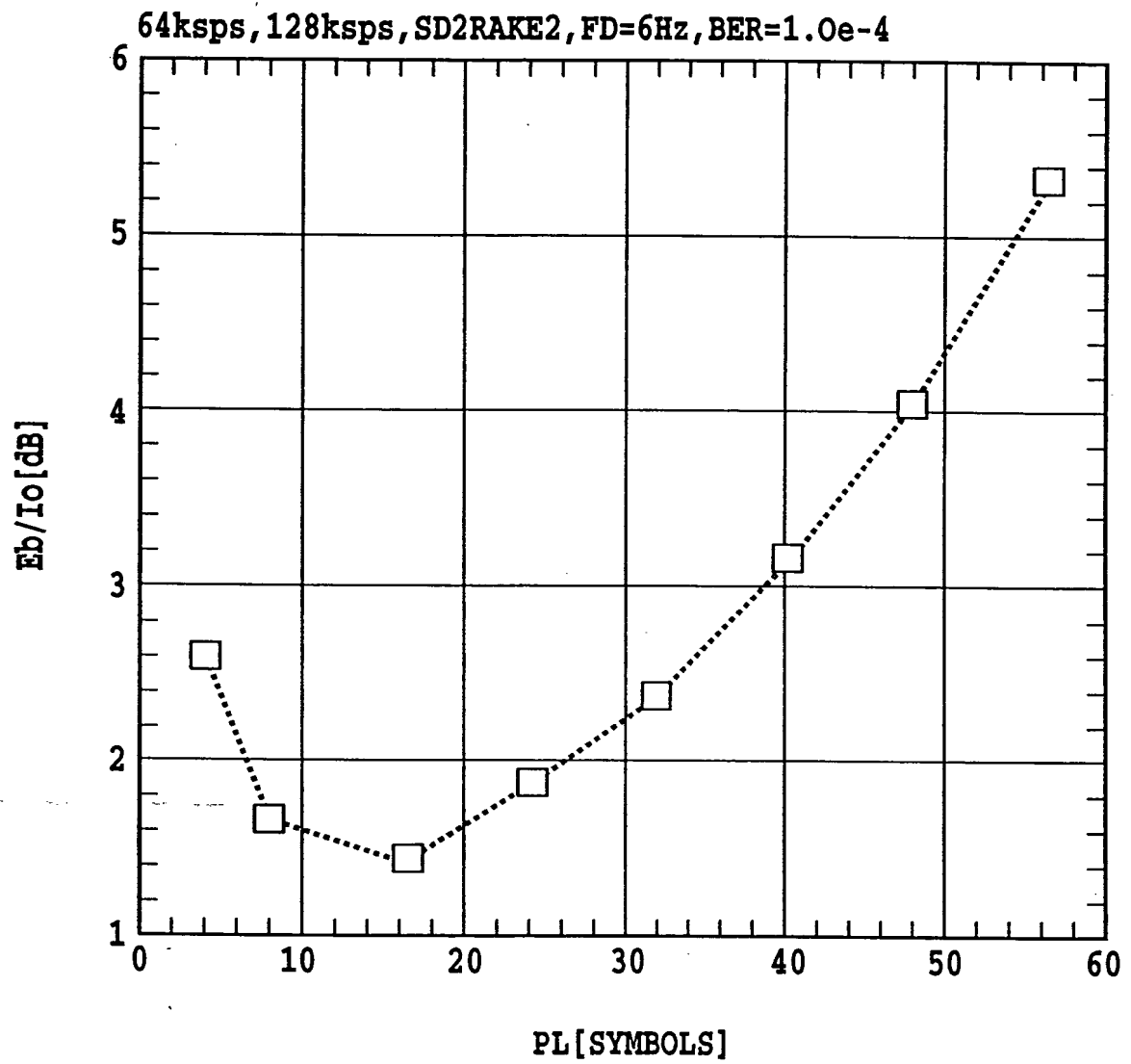


FIG.6

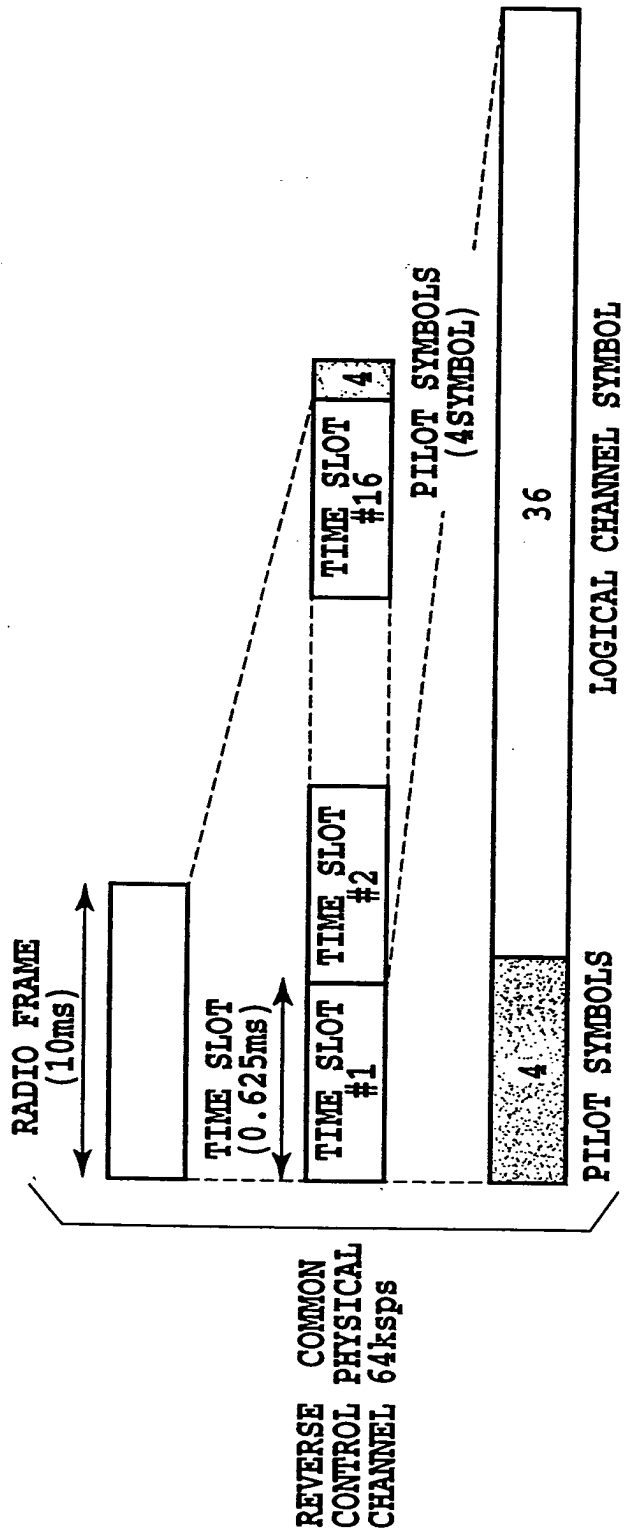


FIG.7A

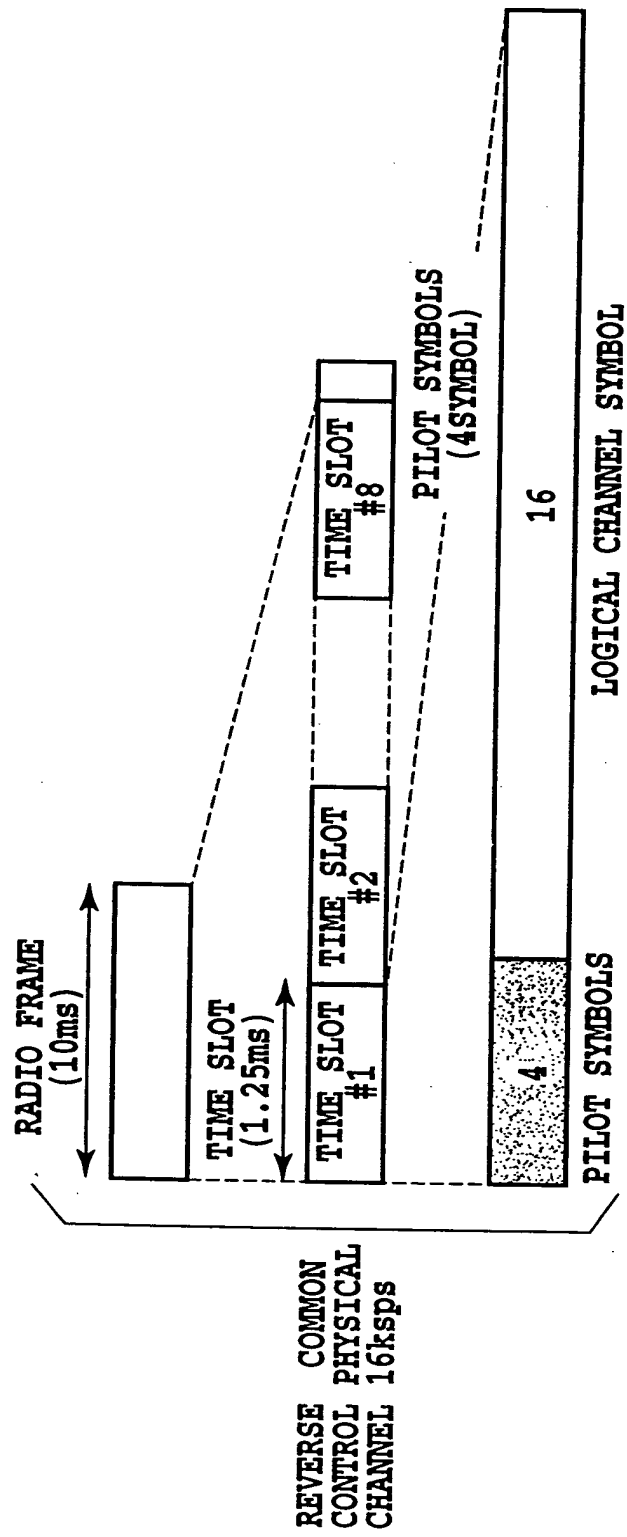


FIG.7B

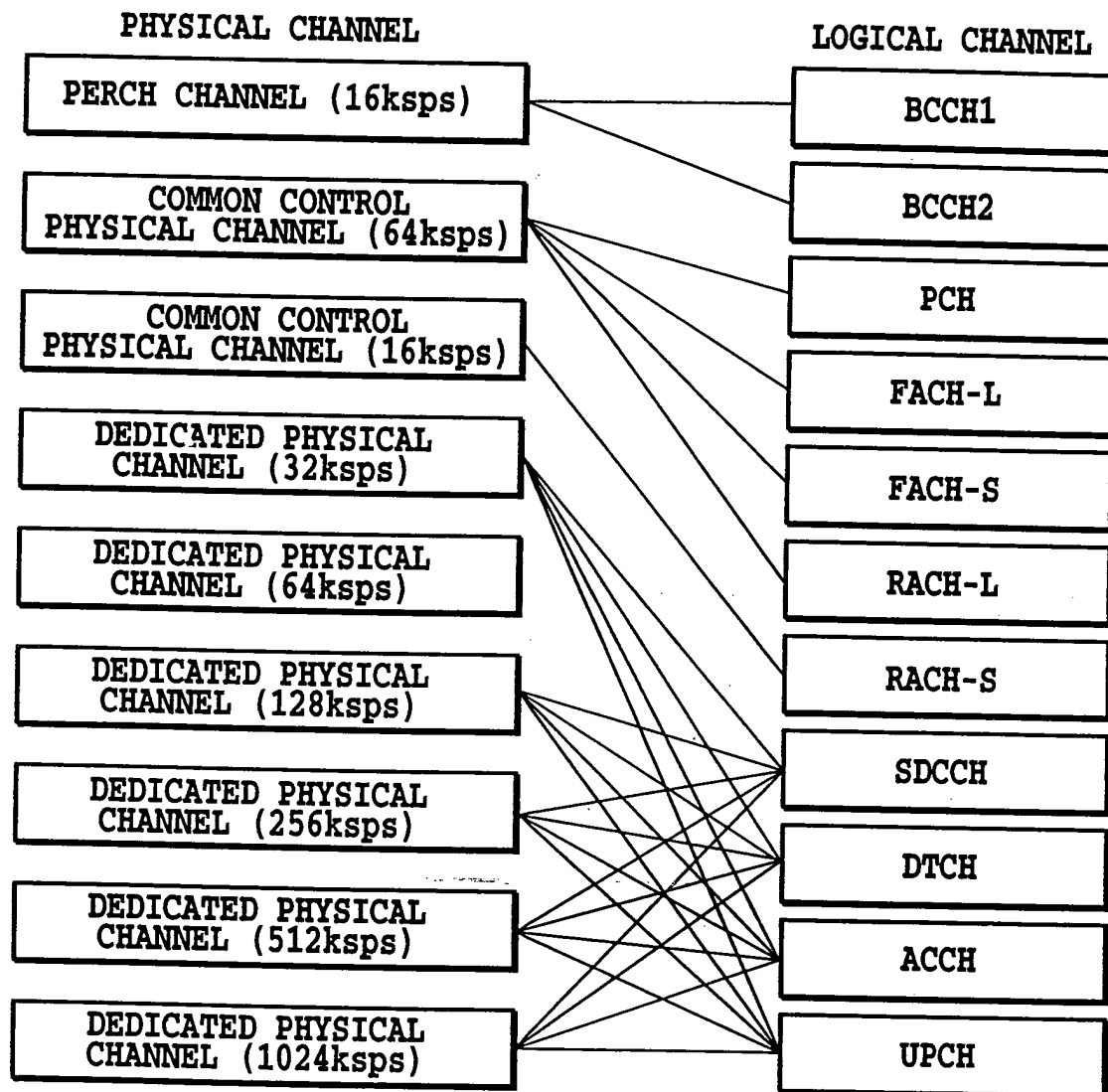


FIG.8

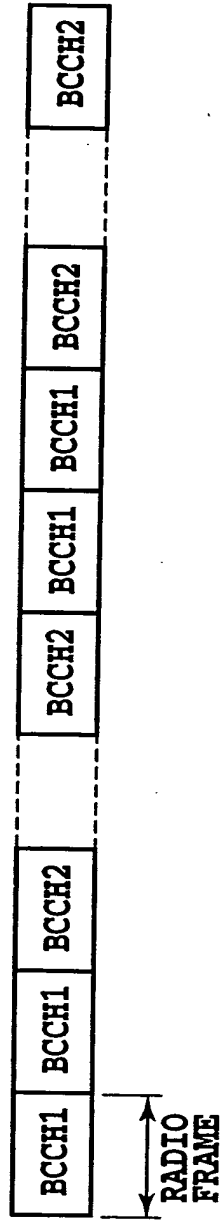


FIG.9

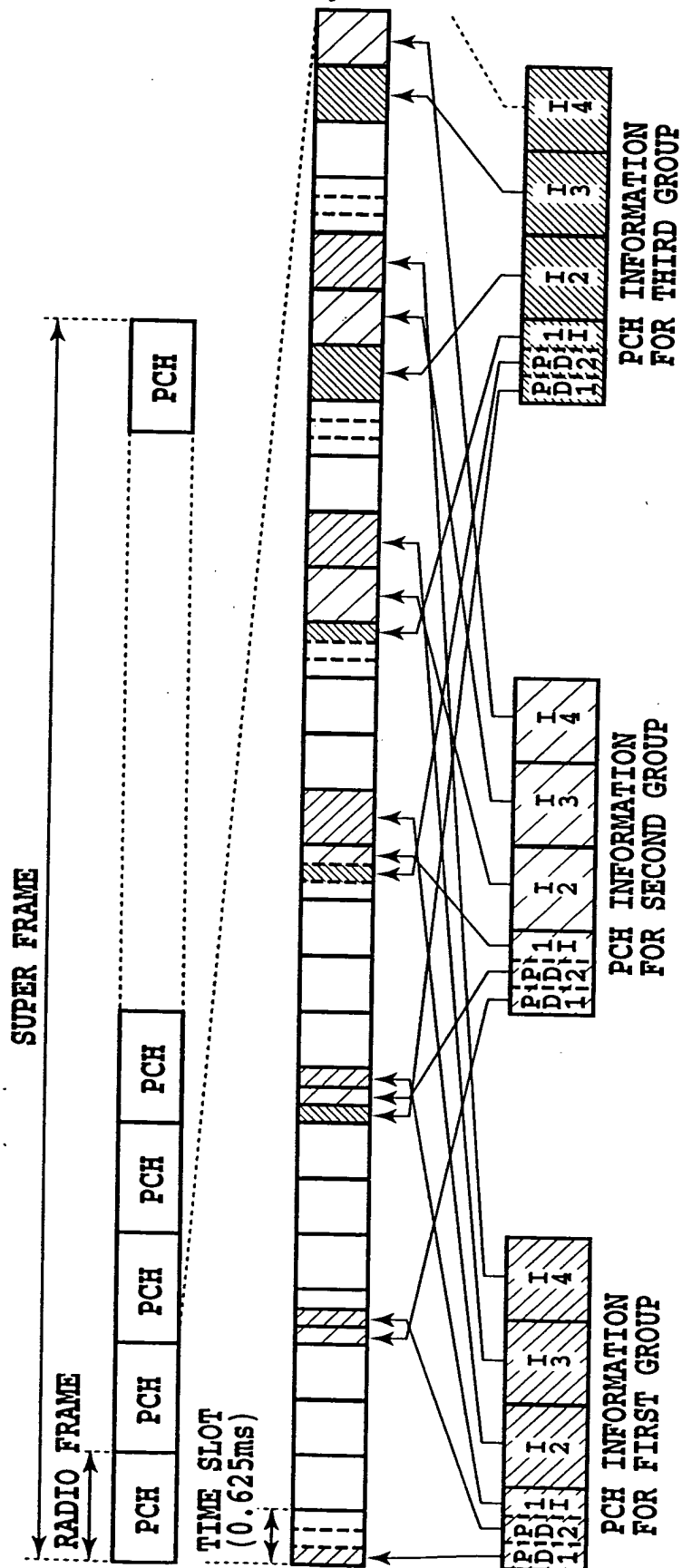


FIG.10

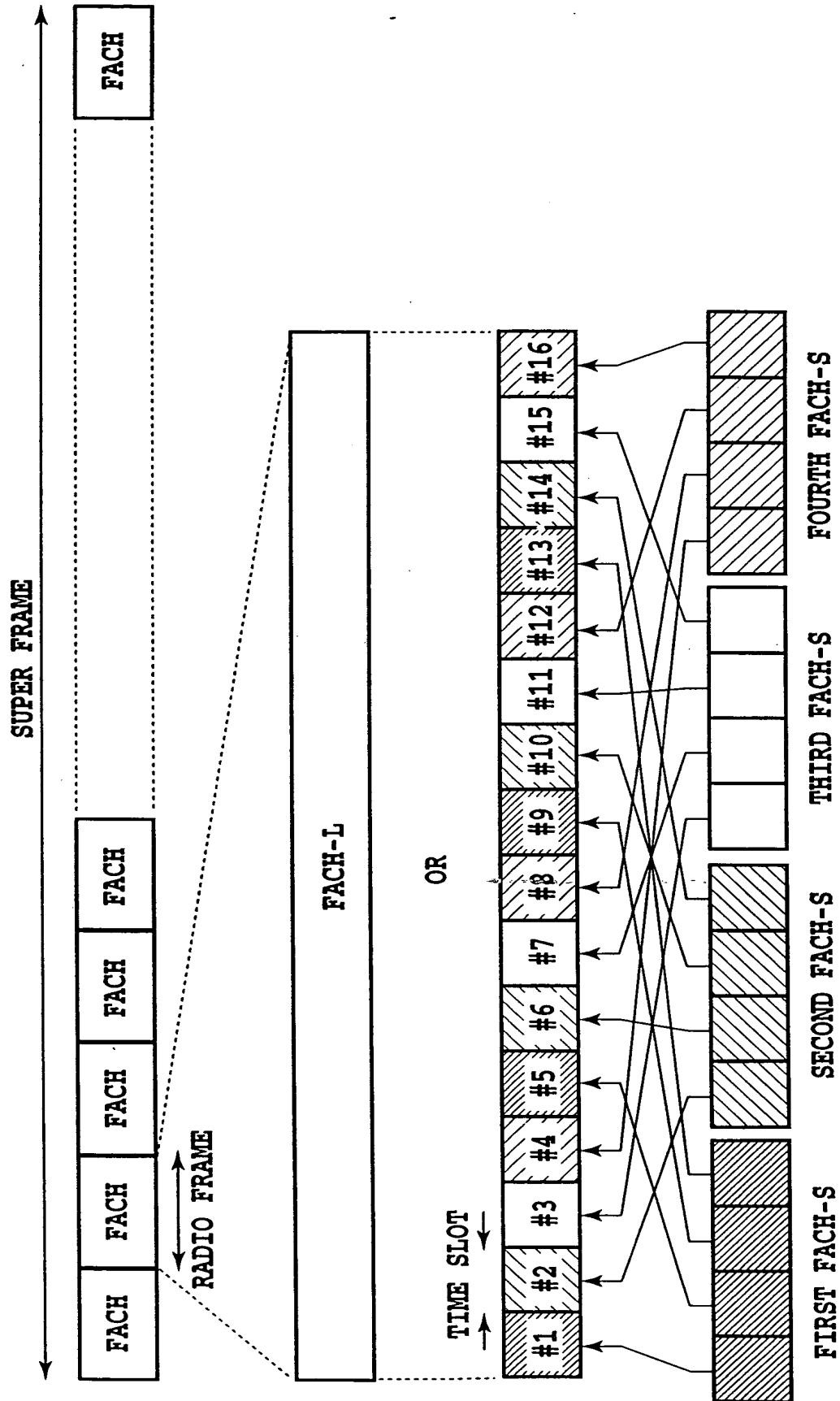


FIG.11

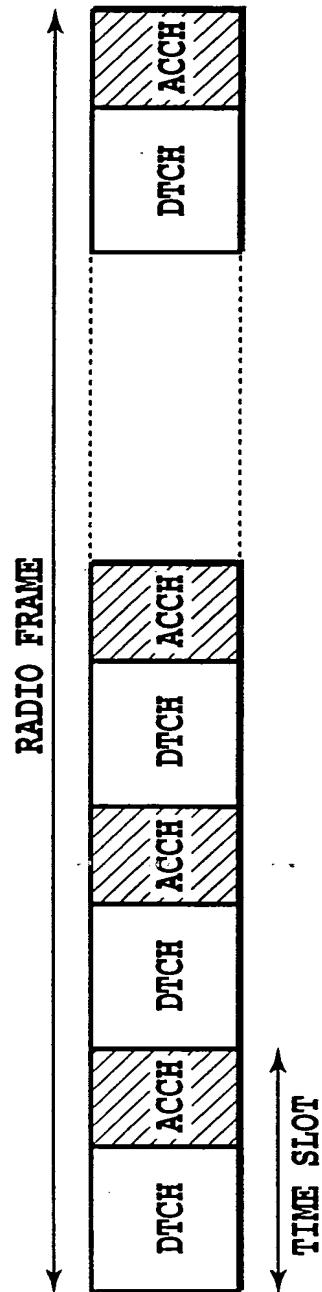
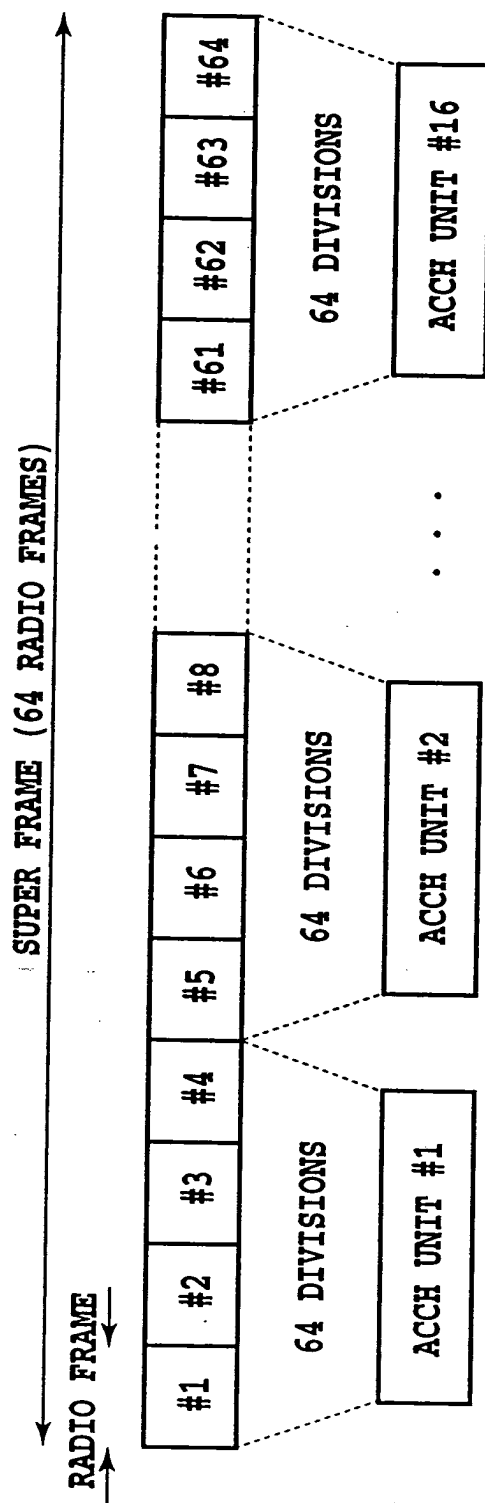
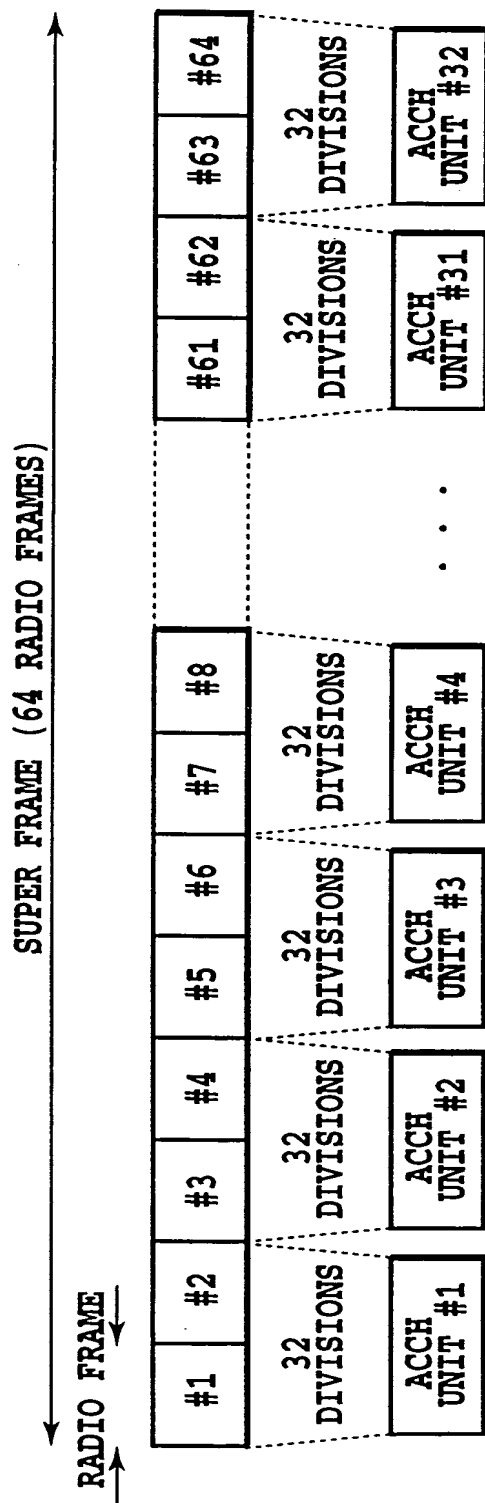


FIG.12



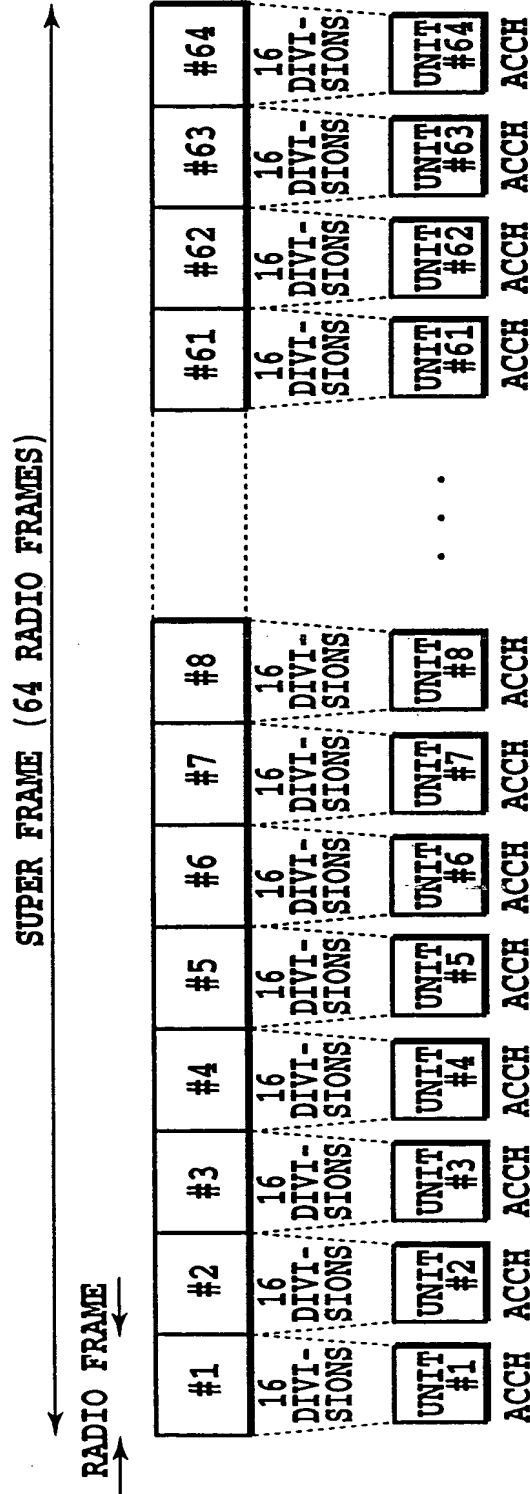
MAPPING INTO 32 OR 64kps DEDICATED PHYSICAL CHANNEL

FIG.13A



MAPPING INTO 128kSPS DEDICATED PHYSICAL CHANNEL

FIG. 13B



MAPPING INTO 256ksps DEDICATED PHYSICAL CHANNEL

FIG.13C

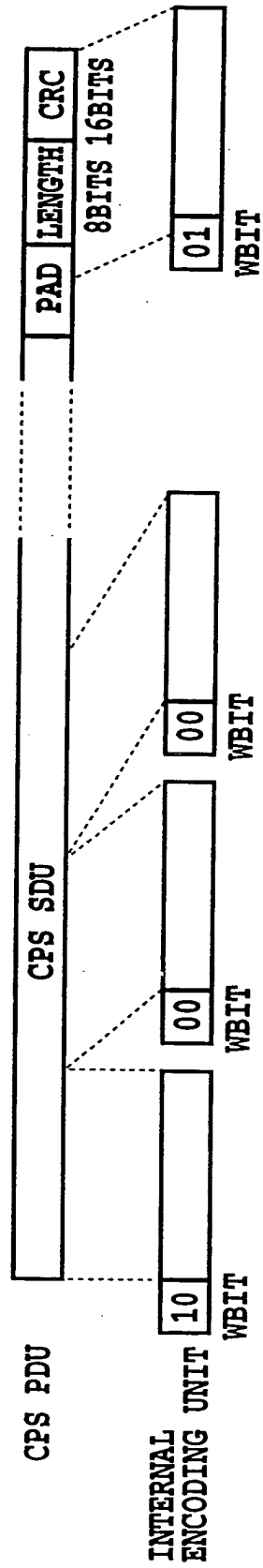


FIG.14

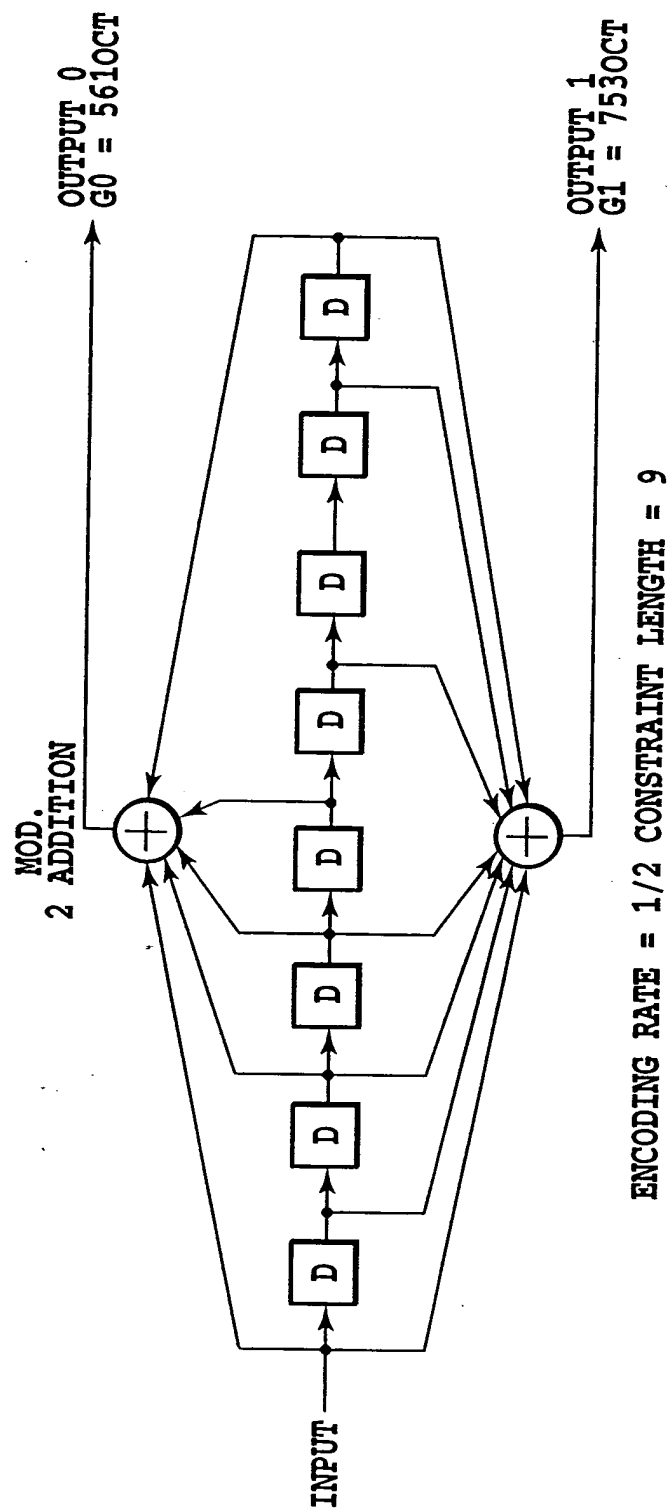
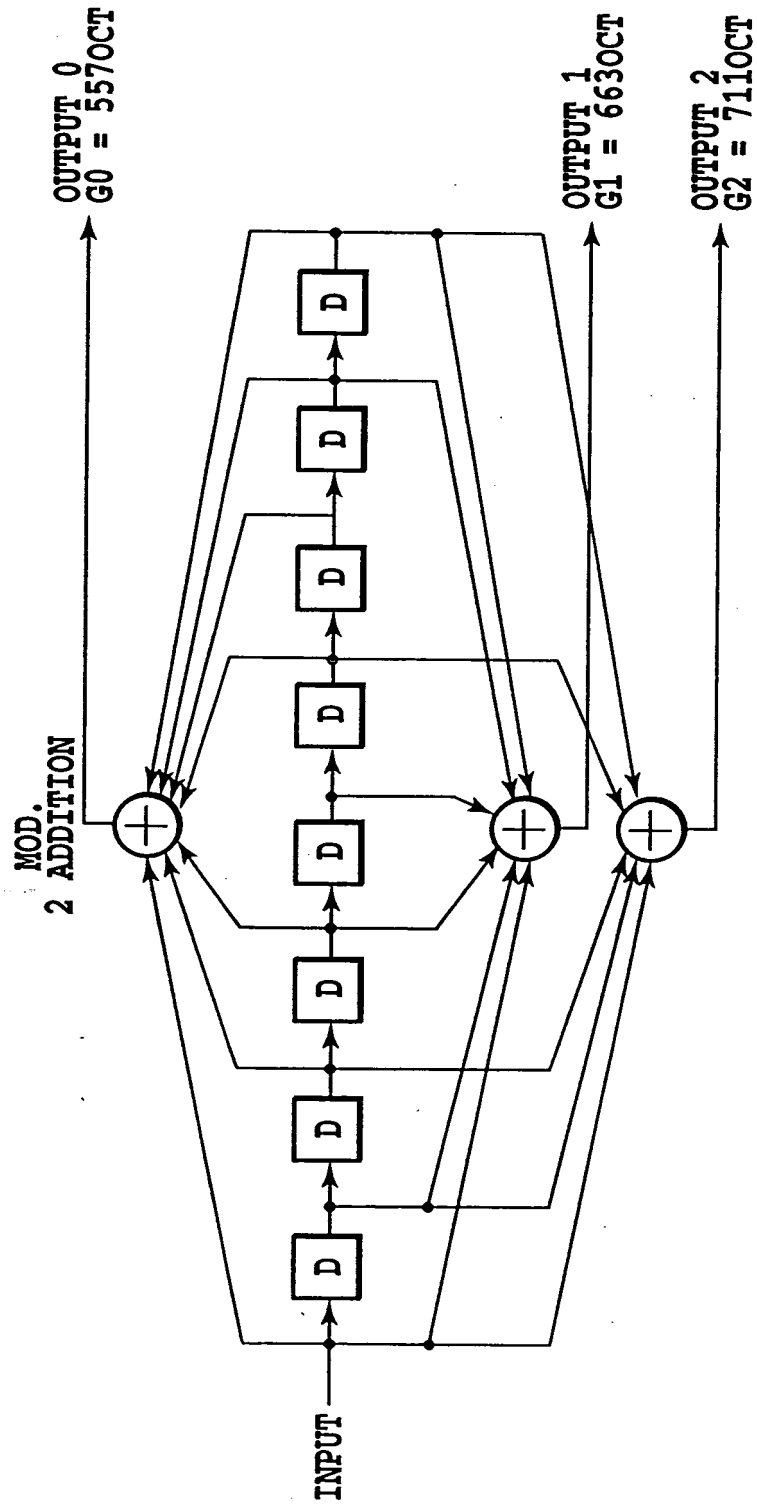


FIG.15A



ENCODING RATE = 1/3 CONSTRAINT LENGTH = 9

FIG.15B

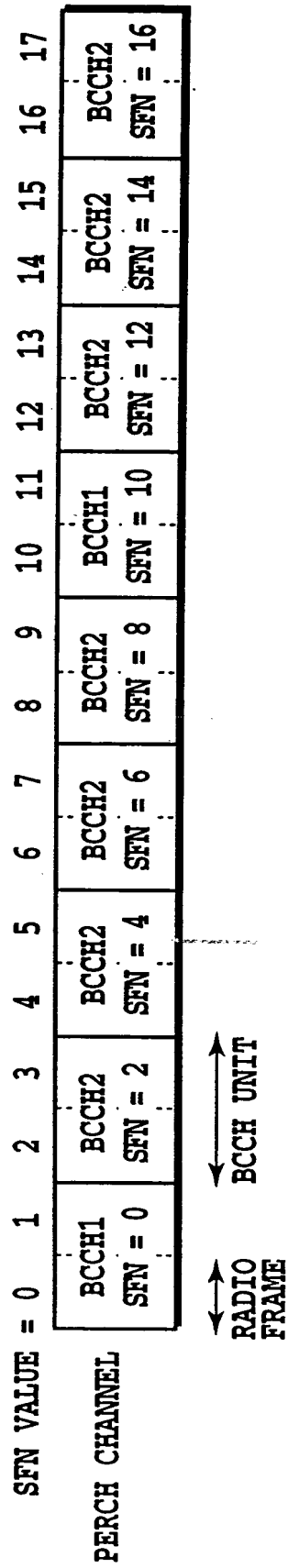


FIG.16

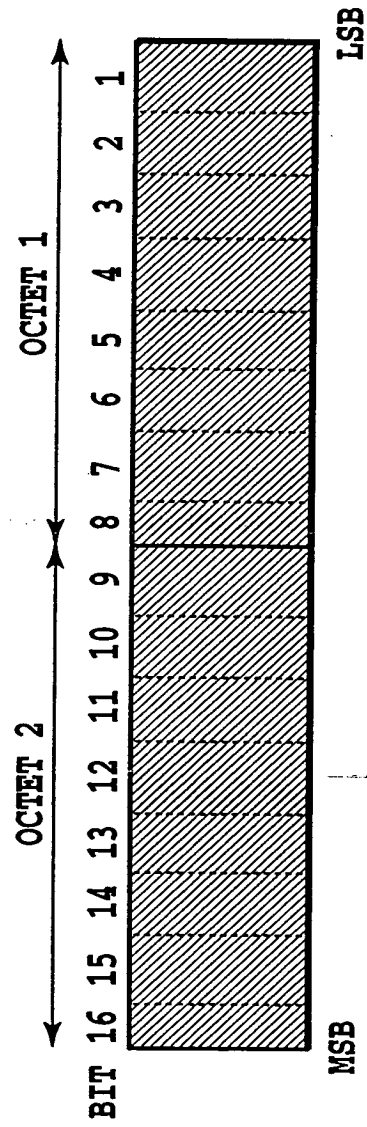


FIG.17

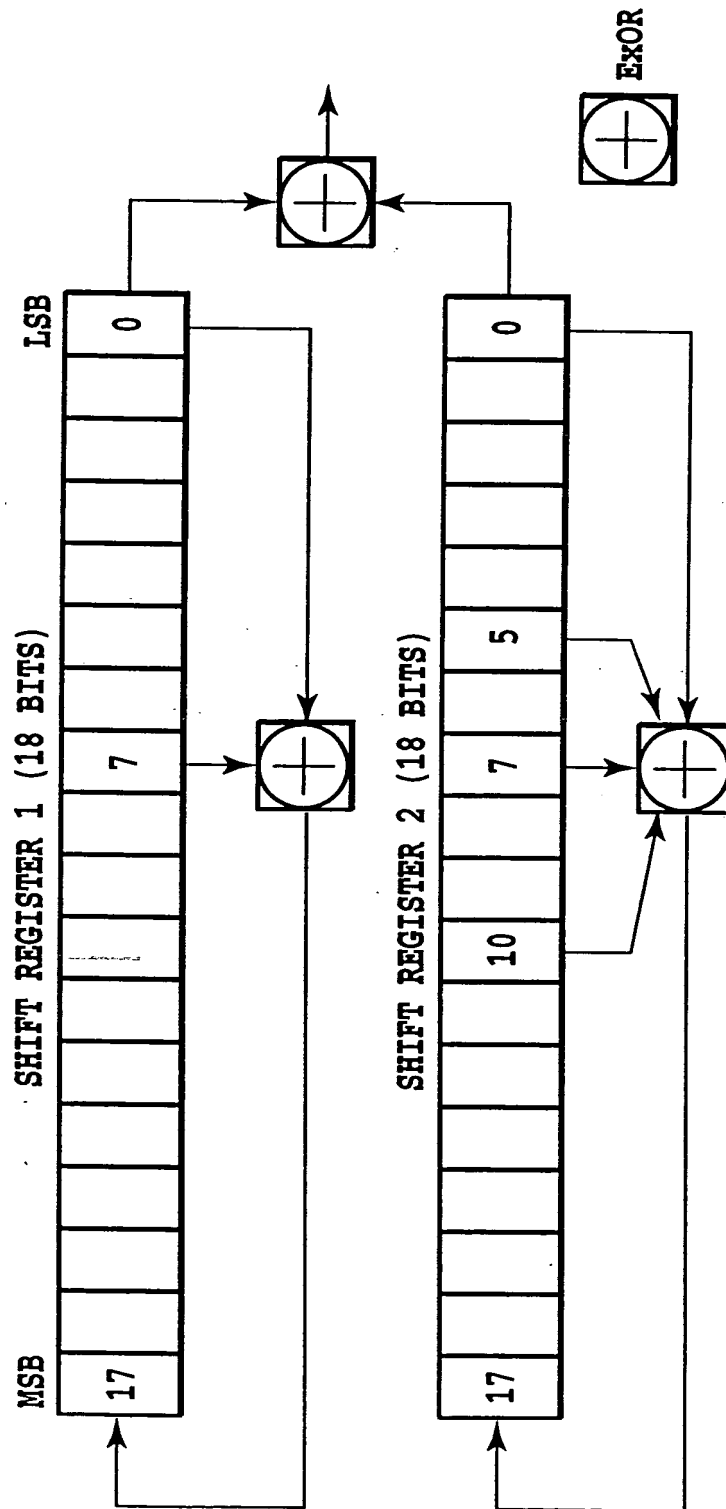


FIG.18

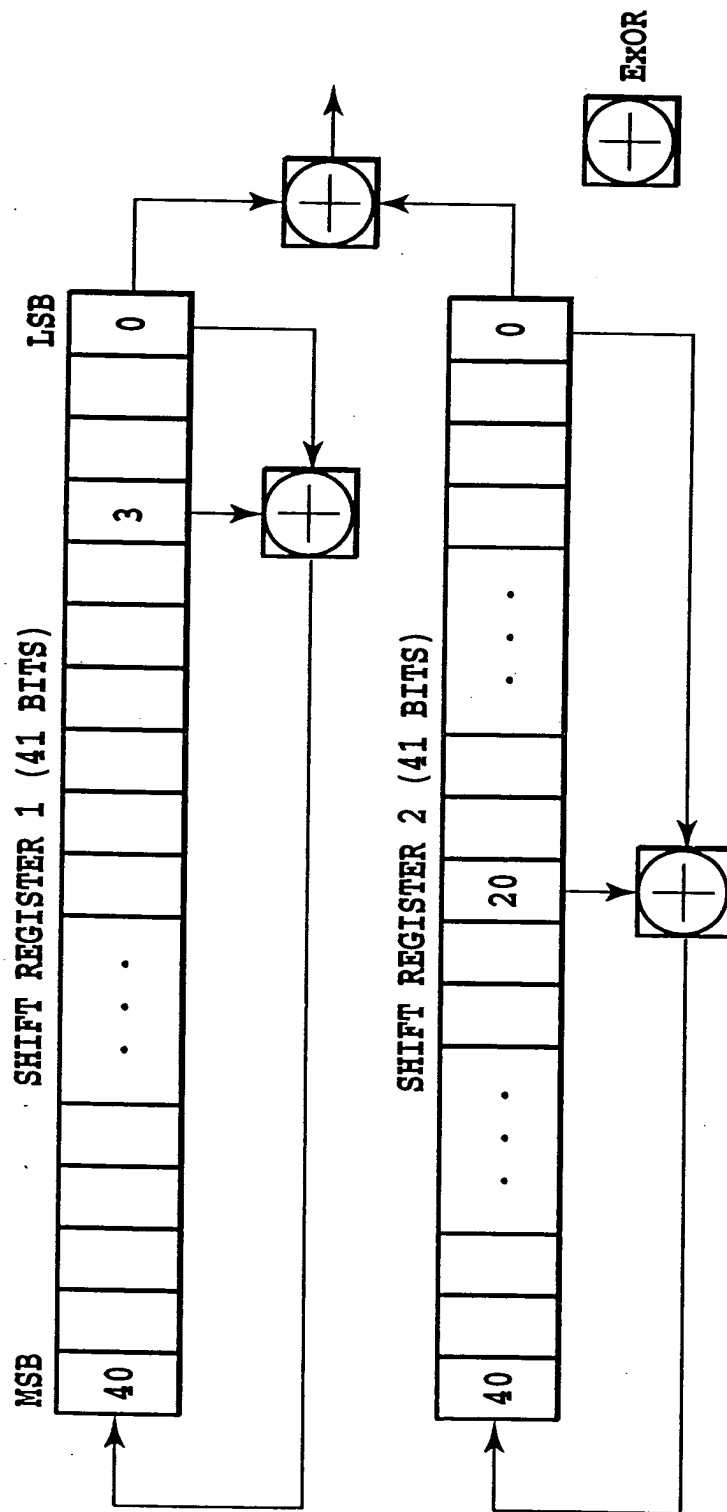


FIG.19

$$C_0(0)=1$$

$$\begin{bmatrix} C_1(0) \\ C_1(1) \end{bmatrix} = \begin{bmatrix} C_0(0) & C_0(0) \\ C_0(0) & \overline{C_0(0)} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix}$$

$$\begin{bmatrix} C_2(0) \\ C_2(1) \\ C_2(2) \\ C_2(3) \end{bmatrix} = \begin{bmatrix} C_1(0) & C_1(0) \\ C_1(0) & \overline{C_1(0)} \\ C_1(1) & C_1(1) \\ C_1(1) & \overline{C_1(1)} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix}$$

$$\vdots$$

$$\begin{bmatrix} C_{n+1}(0) \\ C_{n+1}(1) \\ C_{n+1}(2) \\ C_{n+1}(3) \\ \vdots \\ C_{n+1}(2^{n+1}-2) \\ C_{n+1}(2^{n+1}-1) \end{bmatrix} = \begin{bmatrix} C_n(0) & C_n(0) \\ C_n(0) & \overline{C_n(0)} \\ C_n(1) & C_n(1) \\ C_n(1) & \overline{C_n(1)} \\ \vdots & \vdots \\ C_n(2^{n-1}) & \overline{C_n(2^{n-1})} \\ C_n(2^{n-1}) & \overline{C_n(2^{n-1})} \end{bmatrix}$$

FIG.20

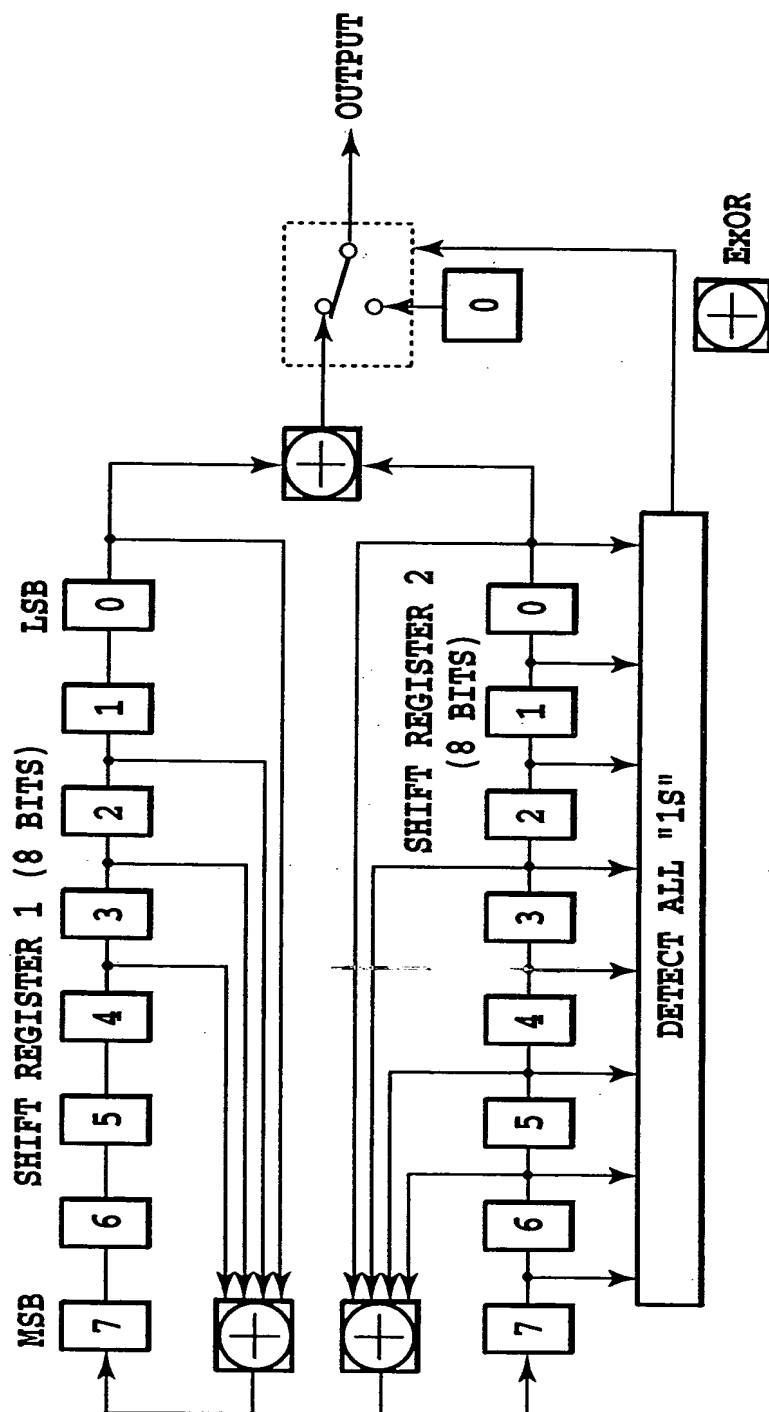


FIG.21

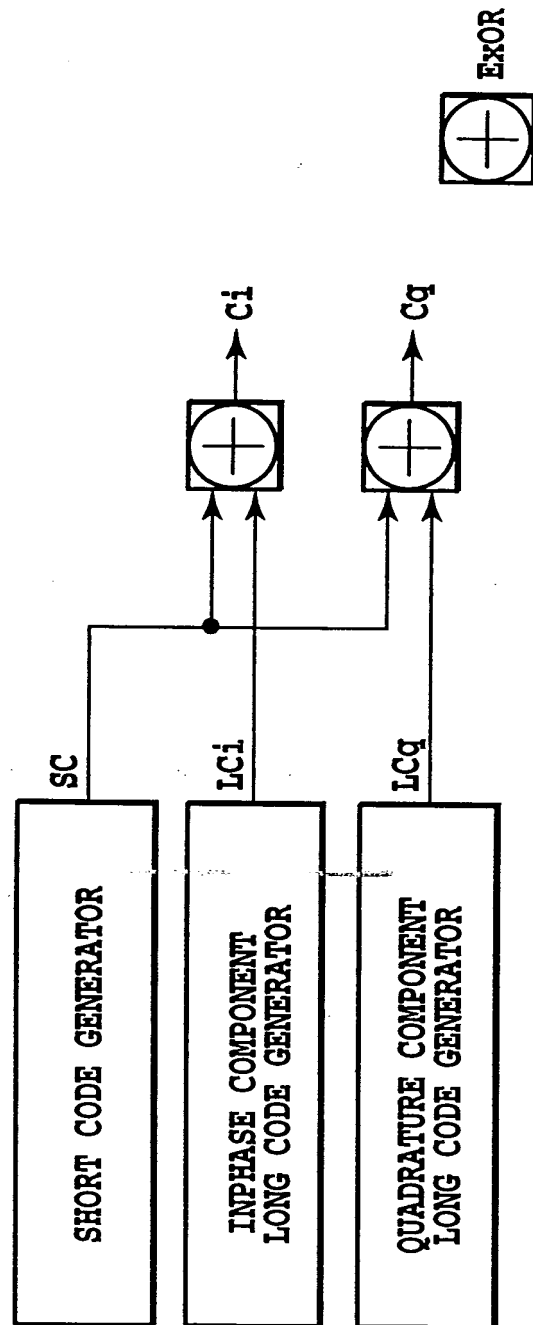


FIG.22

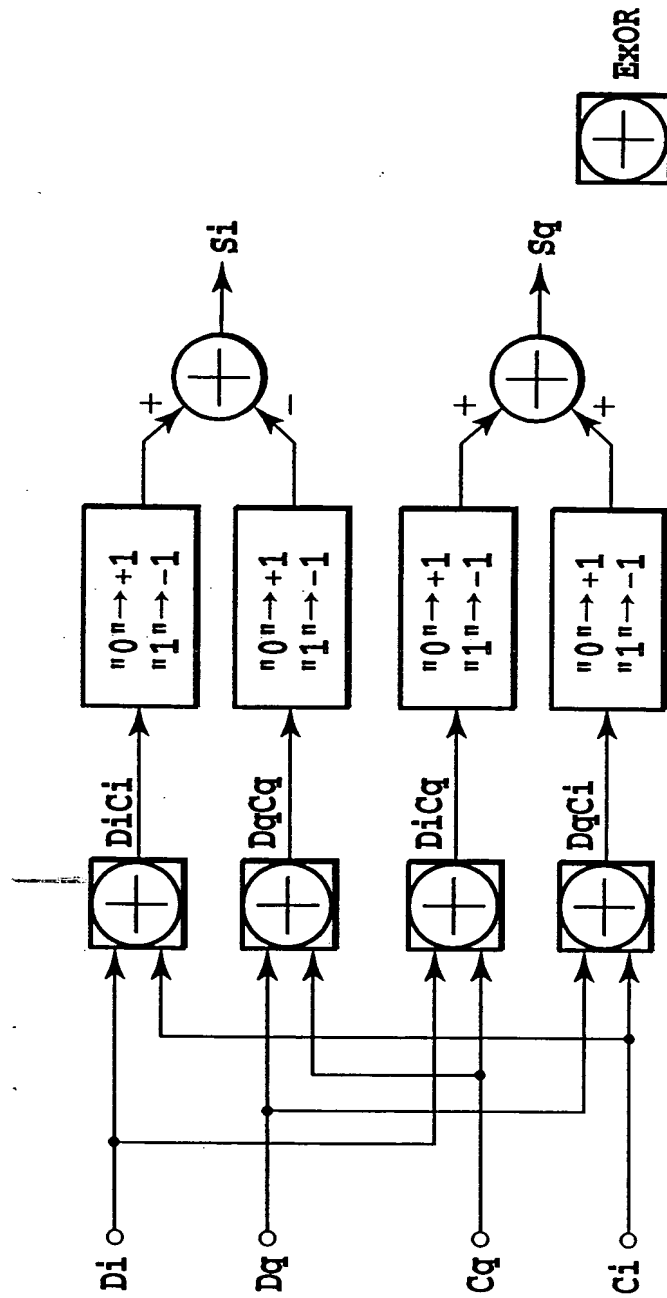


FIG. 23

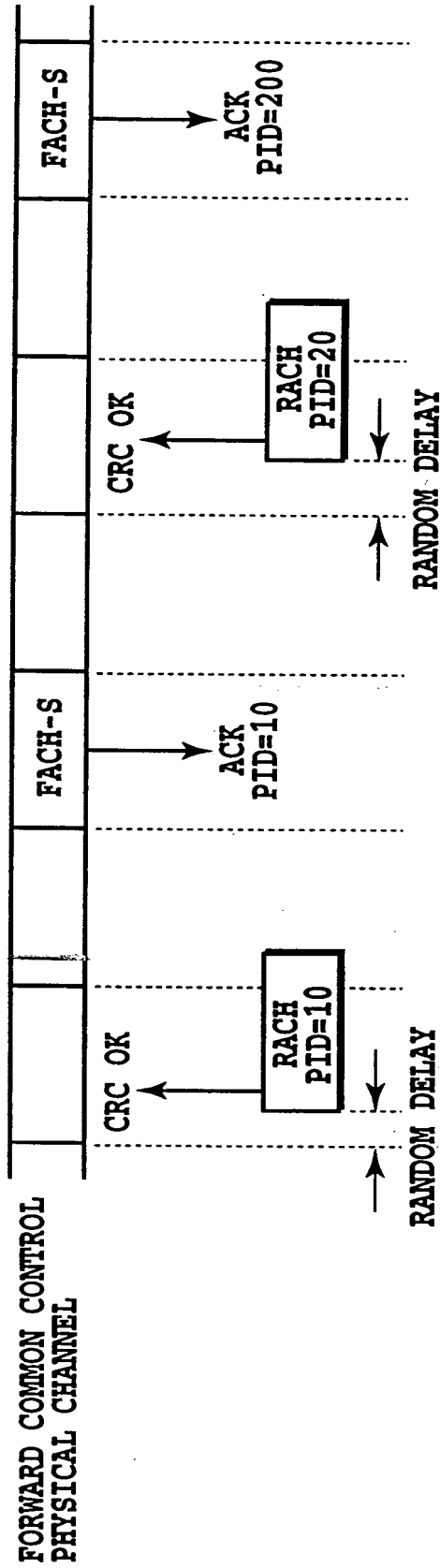


FIG.24

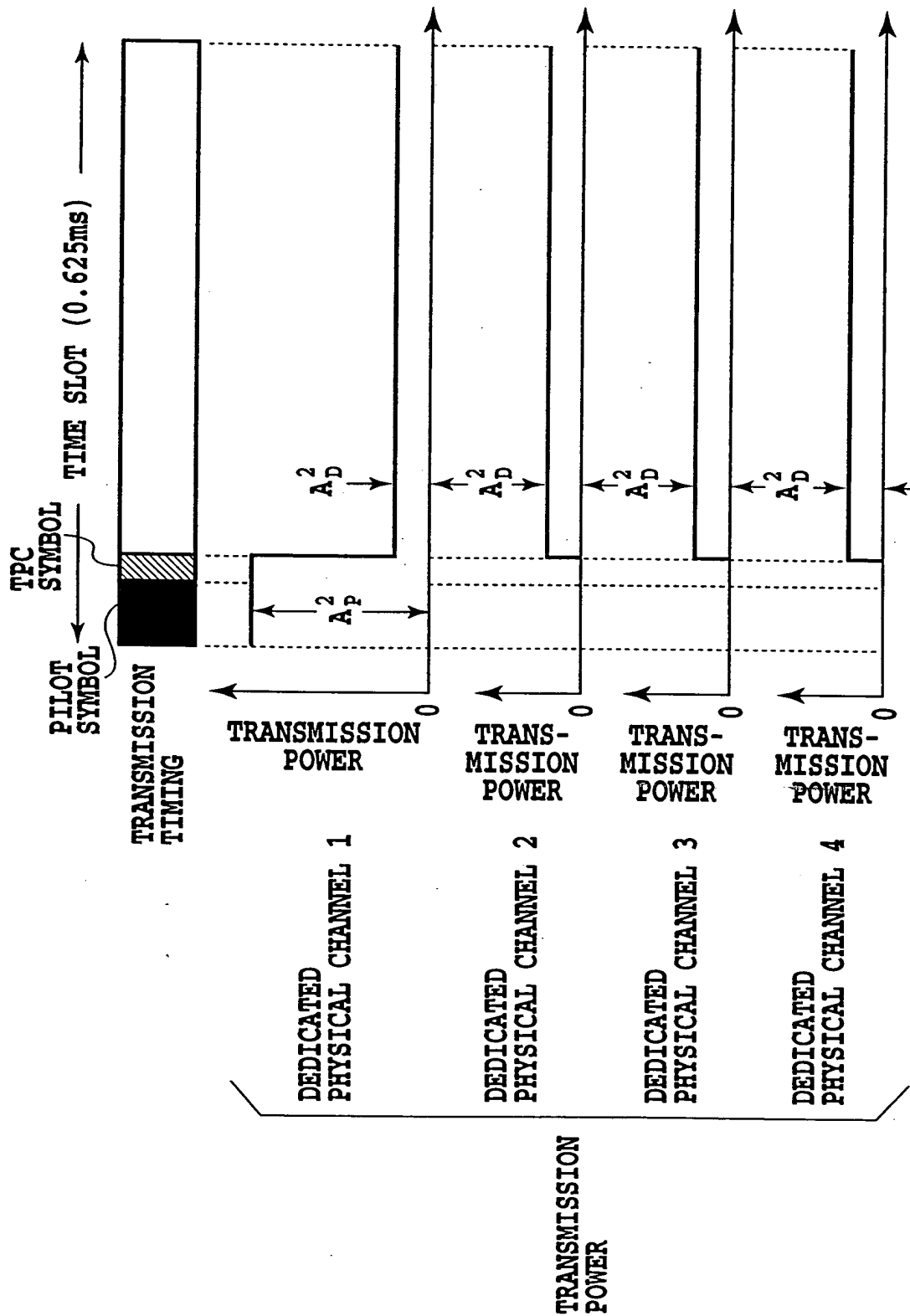


FIG.25

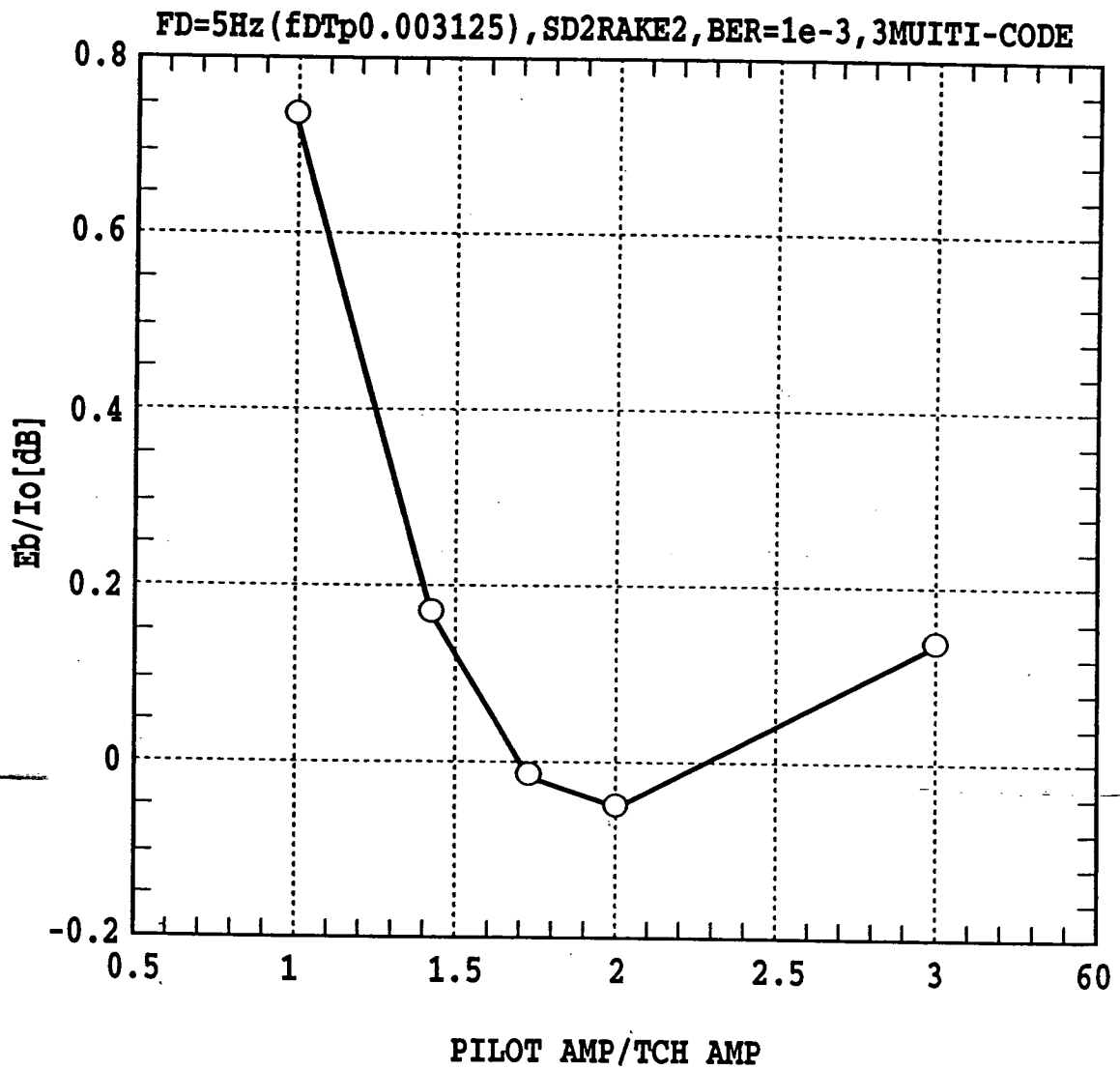


FIG.26

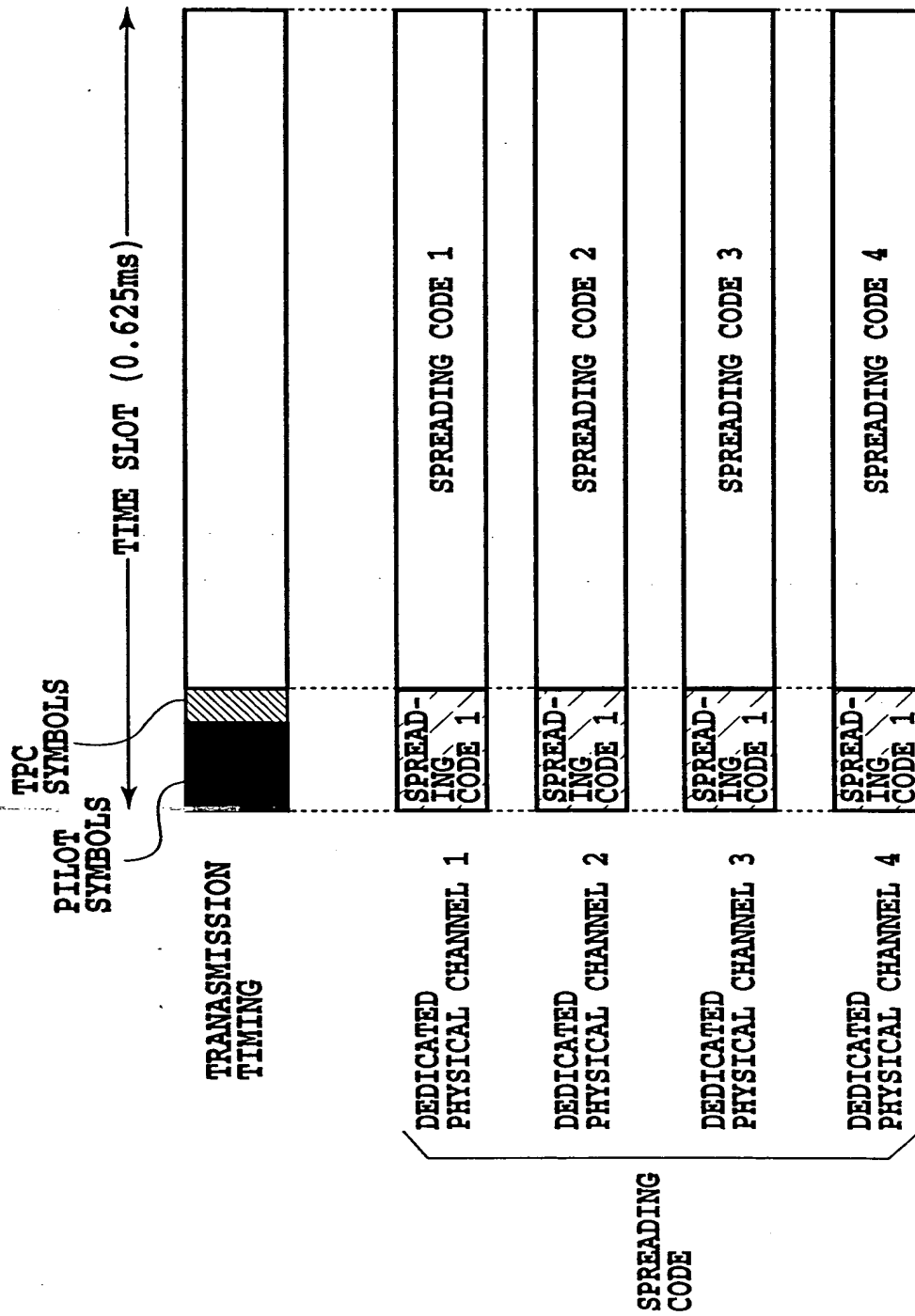


FIG.27

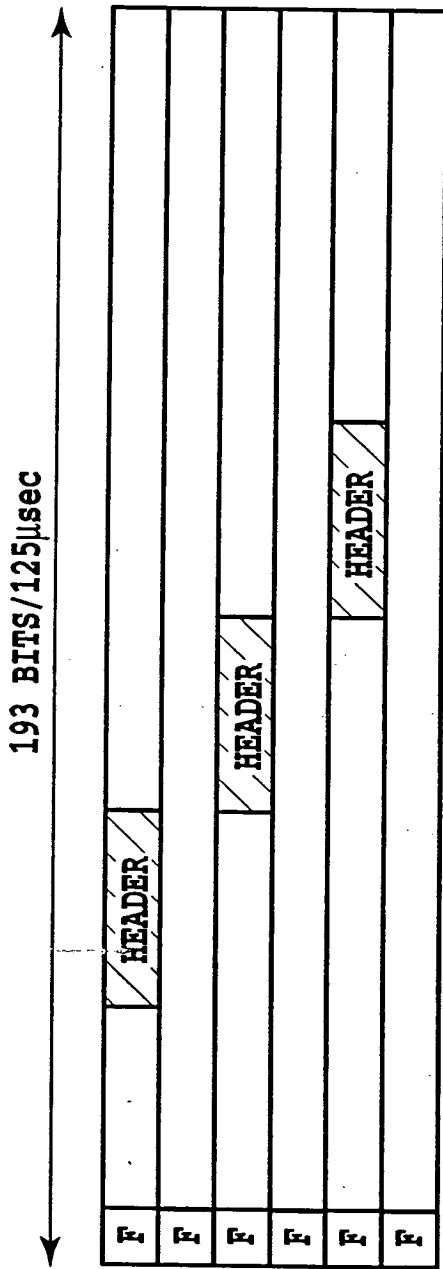
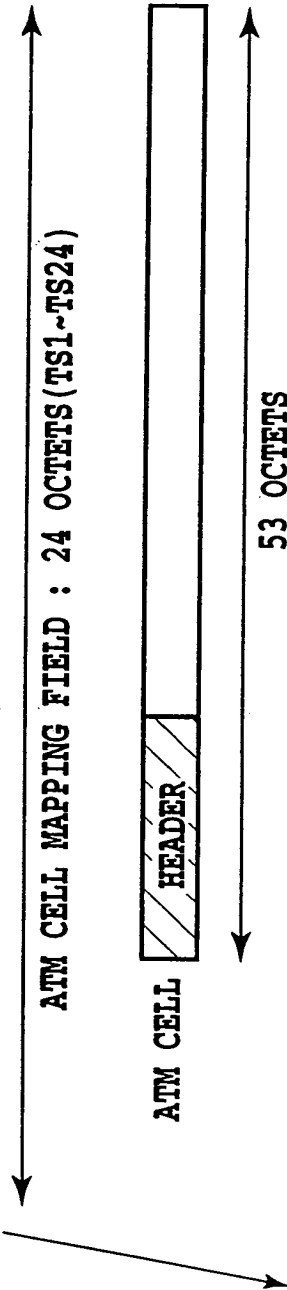


FIG.28A



- PROVIDES F3 OAM FUNCTIONS:
- DETECTION OF LOSS FRAME ALIGNMENT
 - PERFORMANCE MONITORING(CRC-6)
 - TRANSMISSION OF FERF AND LOC
 - PERFORMANCE REPORTING

FIG.28B

TS97,98 : RESERVED FOR SIGNALLING

789 BITS/125 μ s

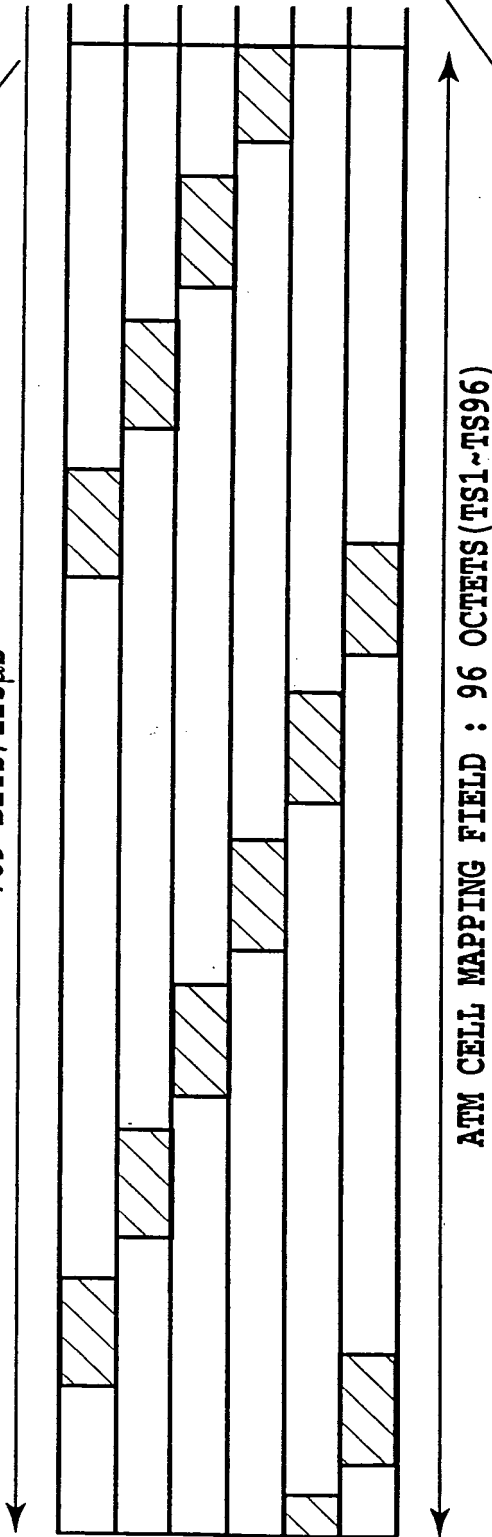


FIG.29A

PROVIDES F3 OAM FUNCTIONS:
 -DETECTION OF LOSS FRAME ALIGNMENT
 -PERFORMANCE MONITORING(CRC-5)
 -TRANSMISSION OF FERF AND LOC
 -PERFORMANCE REPORTING

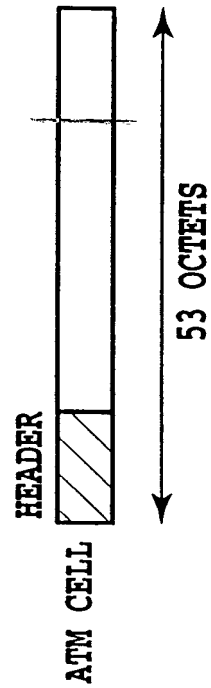
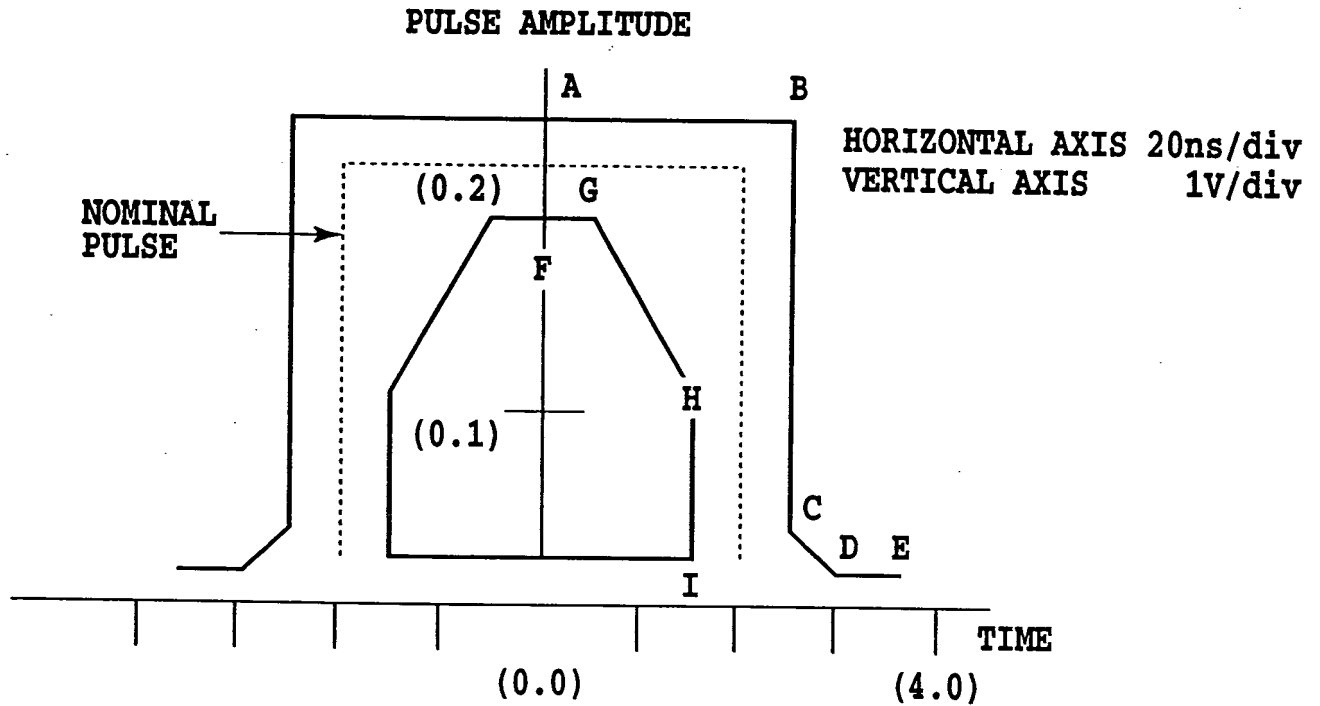


FIG.29B



**COORDINATES OF
INTERSECTION POINTS**

A : (0, 2.3)	F : (0, 1.7)
B : (2.4, 2.3)	G : (0.4, 1.7)
C : (2.4, 1.0)	H : (1.6, 0.9)
D : (3.2, 0.3)	I : (1.6, 0.3)
E : (4.0, 0.3)	

FIG.30

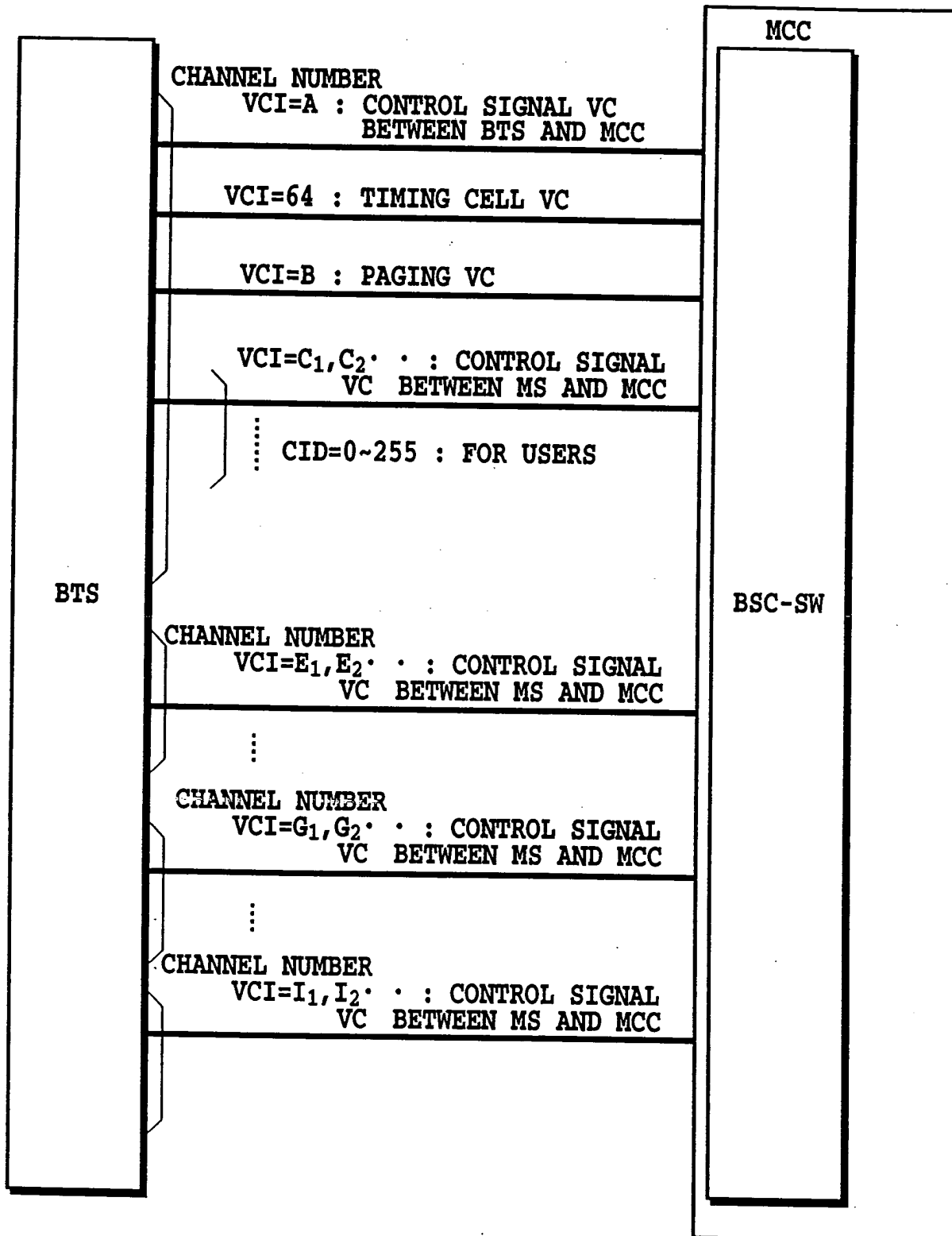


FIG.31

	BIT	8	0	
OCT 1			00H	CELL HEADER
OCT 2			00H	
OCT 3			00H	
OCT 4			01H	
OCT 5			52H	
OCT 6			6AH	
OCT 1			6AH	

FIG.32

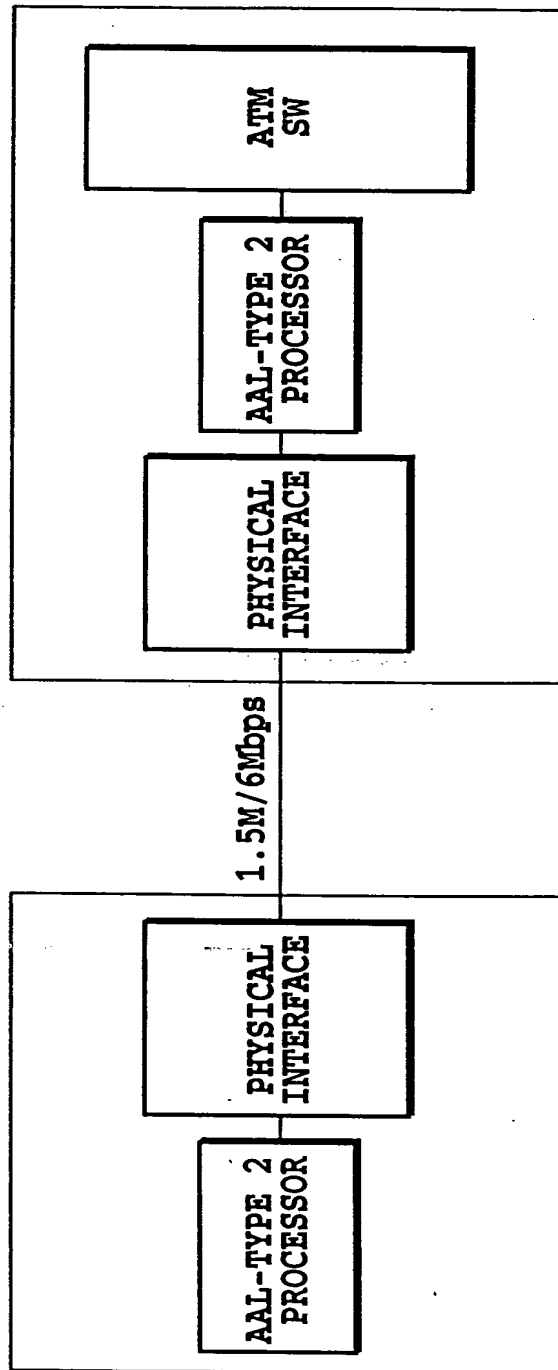


FIG.33A

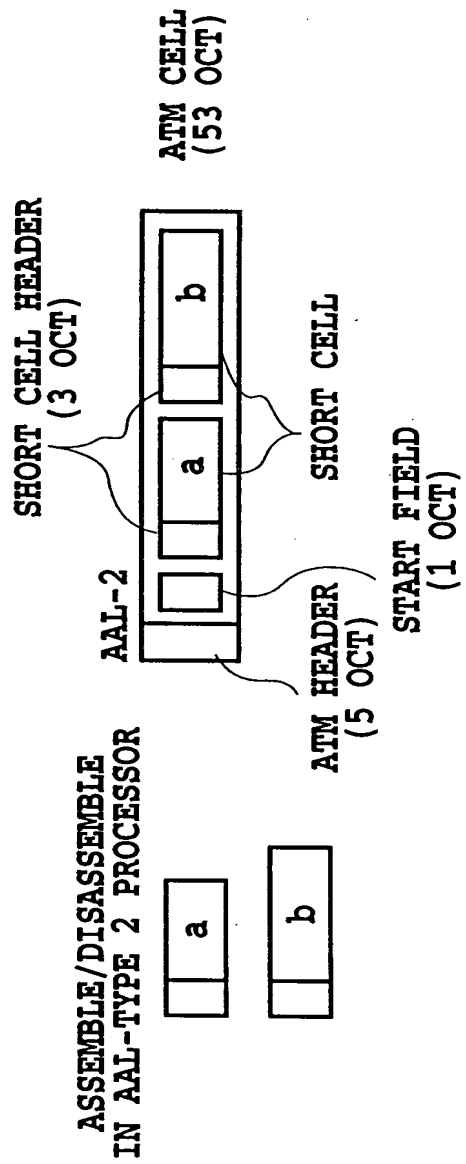


FIG.33B

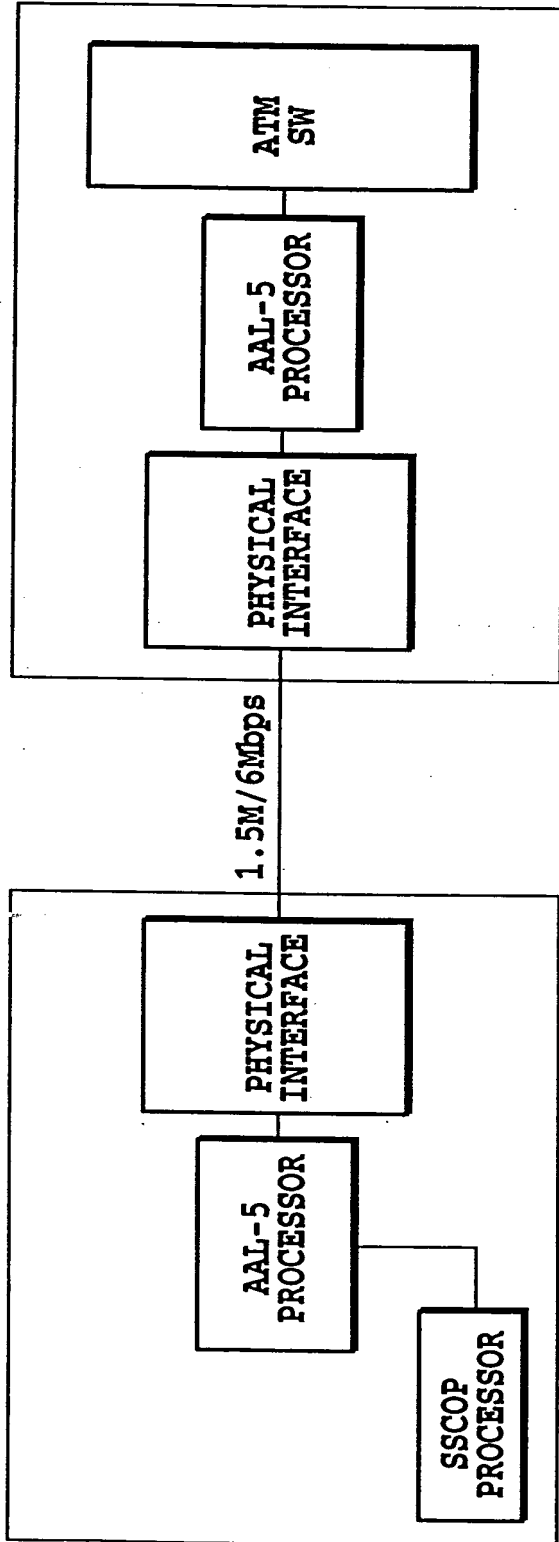


FIG.34A

ASSEMBLE/DISASSEMBLE
IN AAL-5 PROCESSOR

AAL-5

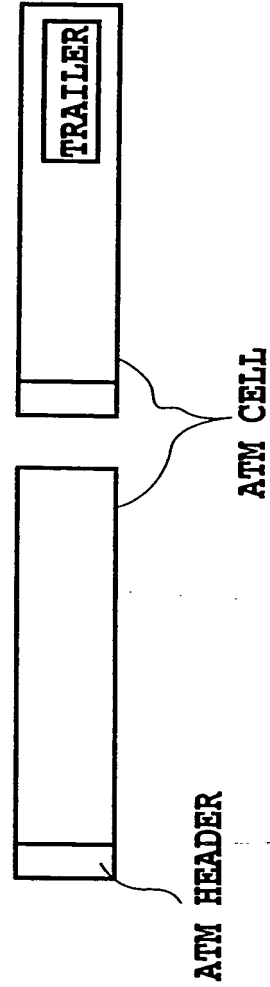
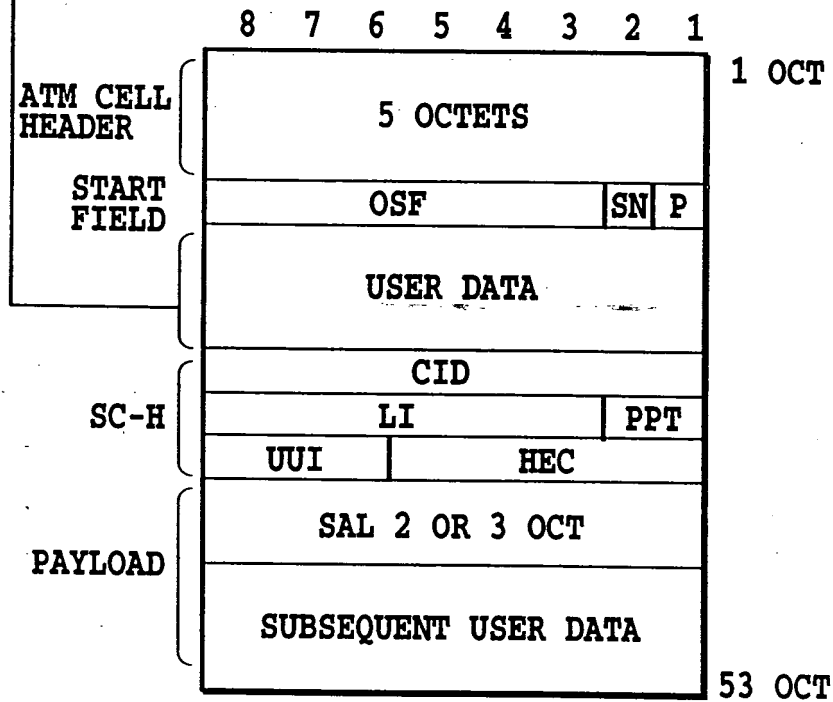
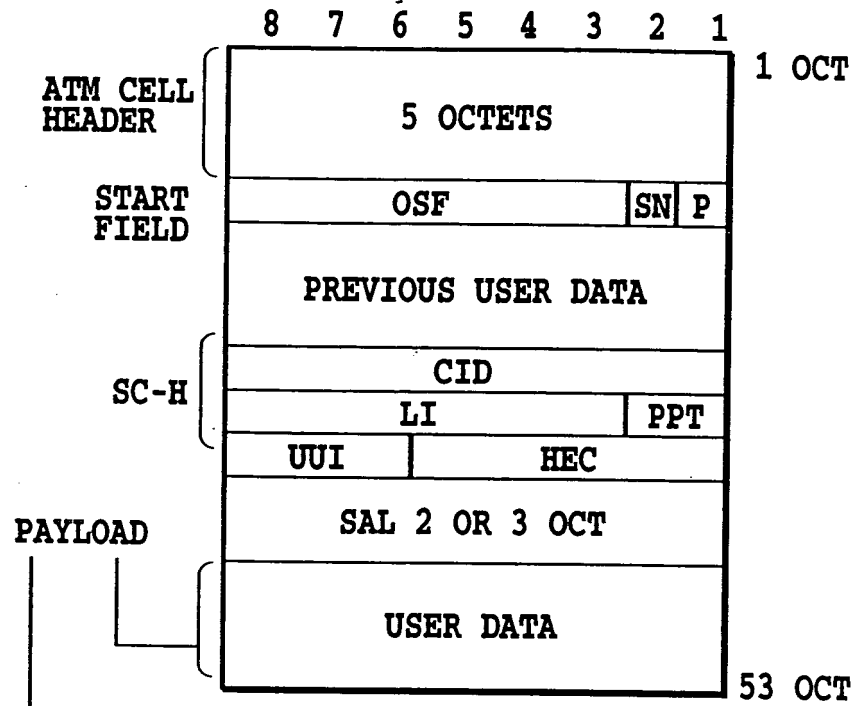


FIG.34B

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- START FIELD (1 OCTET)
- OSF: OFFSET FIELD

FIG.35

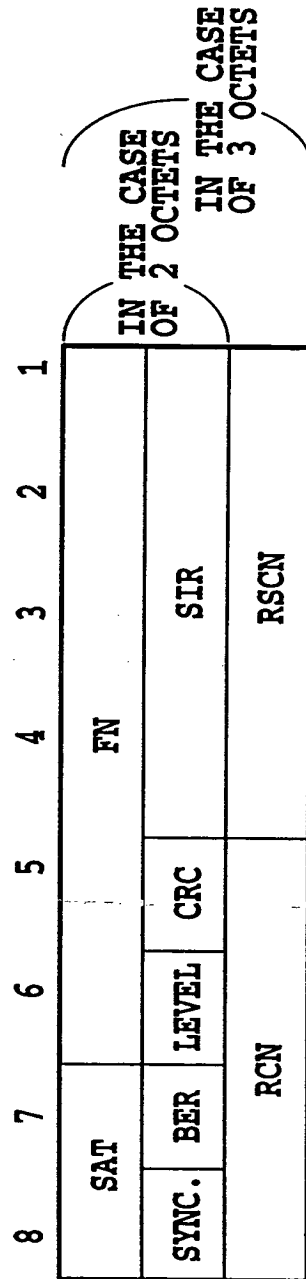


FIG.36

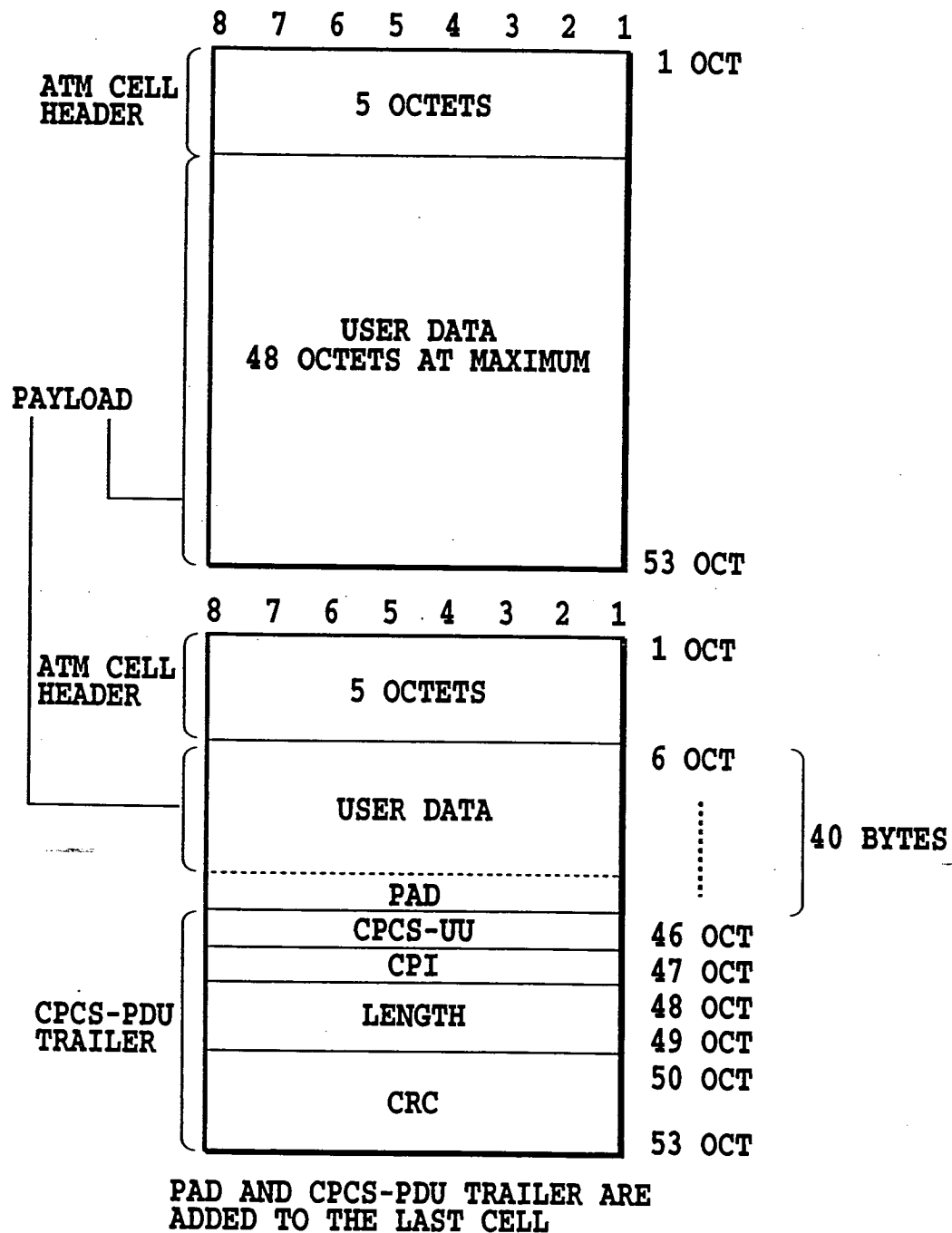


FIG.37

FIG.38

FIG.38A
FIG.38B

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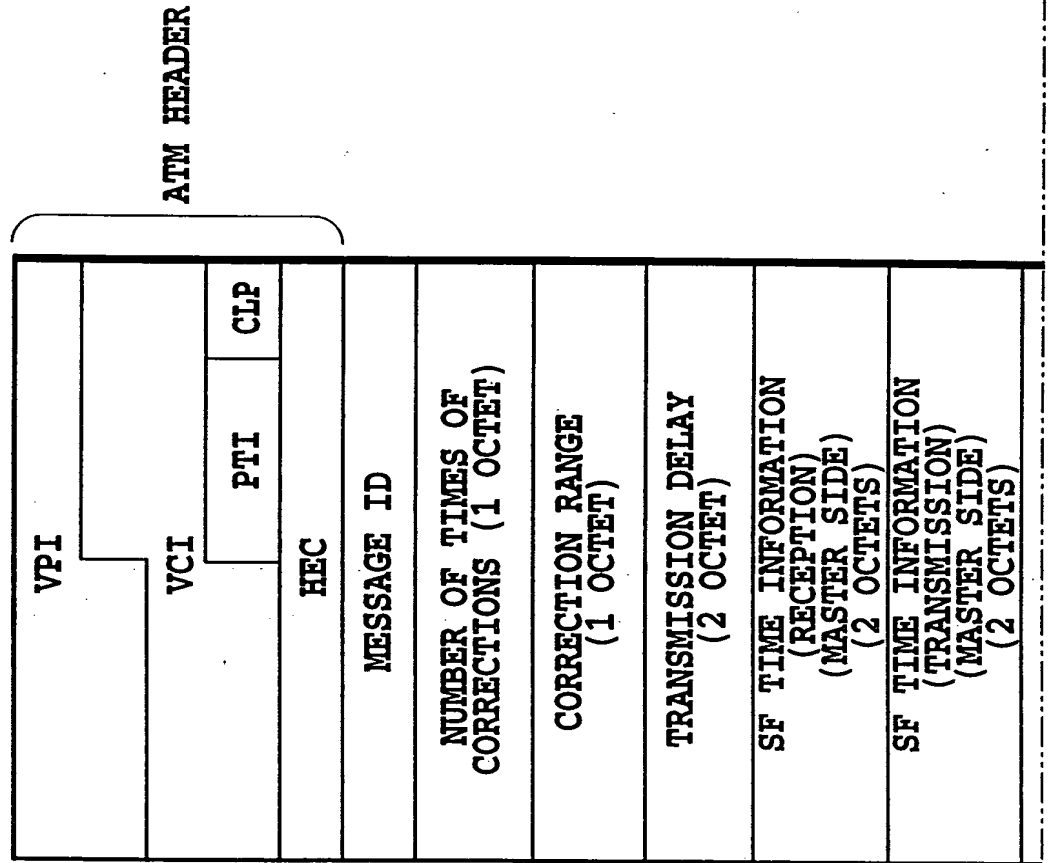


FIG.38A

SF TIME INFORMATION (RECEPTION) (SLAVE SIDE) (2 OCTETS)
SF TIME INFORMATION (TRANSMISSION) (SLAVE SIDE) (2 OCTETS)
SF PHASE SHIFT VALUE (2 OCTETS)
LC COUNTER INFORMATION (RECEPTION) (MASTER SIDE) (3 OCTETS)
LC COUNTER INFORMATION (TRANSMISSION) (MASTER SIDE) (3 OCTETS)
LC COUNTER INFORMATION (RECEPTION) (SLAVE SIDE) (3 OCTETS)
LC COUNTER INFORMATION (TRANSMISSION) (SLAVE SIDE) (3 OCTETS)
LC COUNTER SHIFT VALUE (3 OCTETS)
UNUSED (6A (h))
000000
CRC-10

FIG.38B

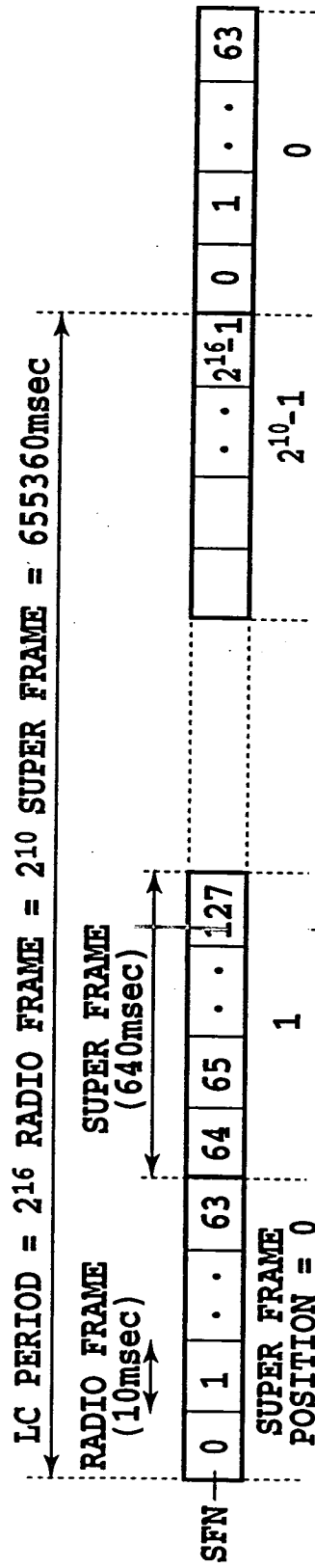


FIG.39

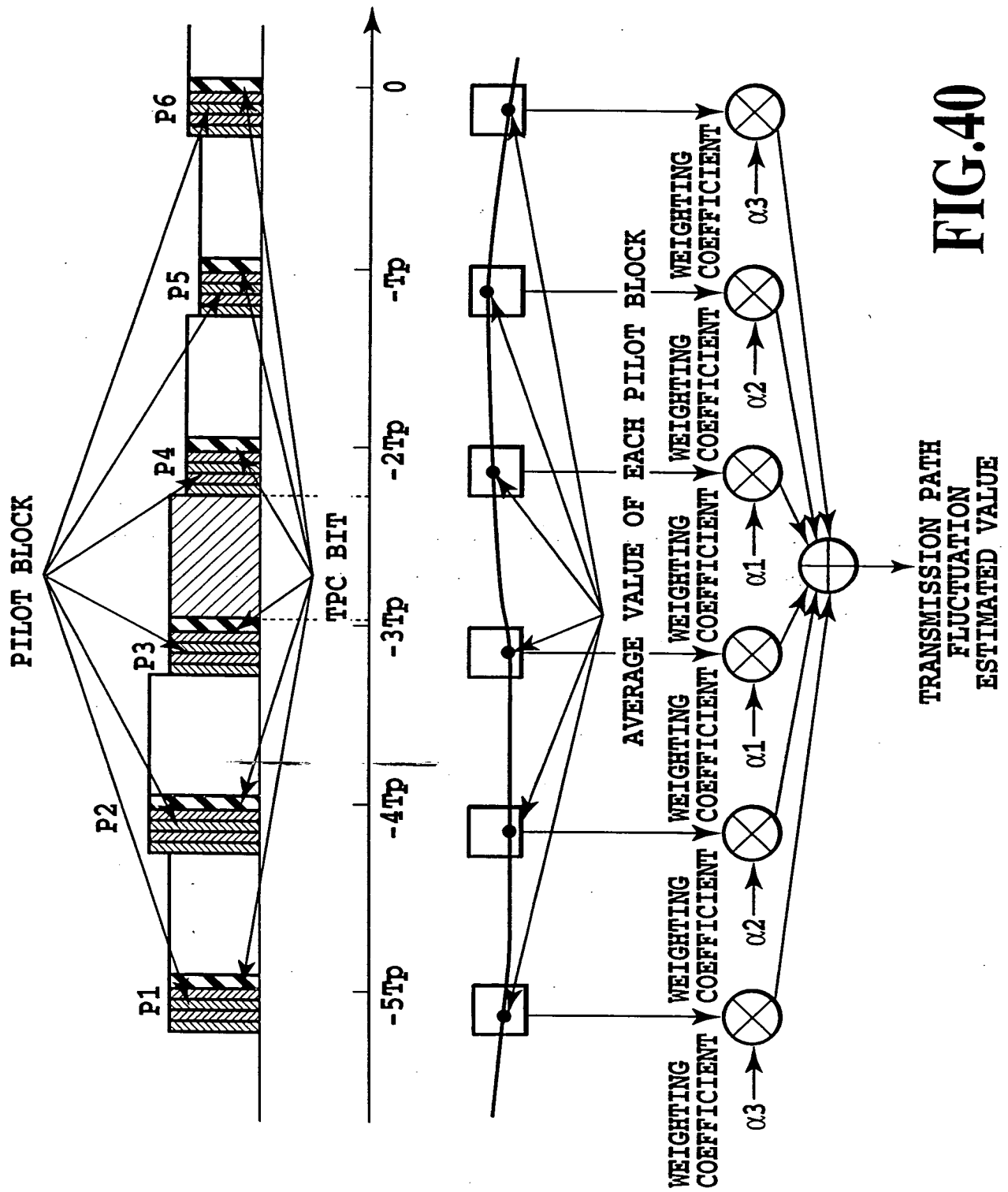
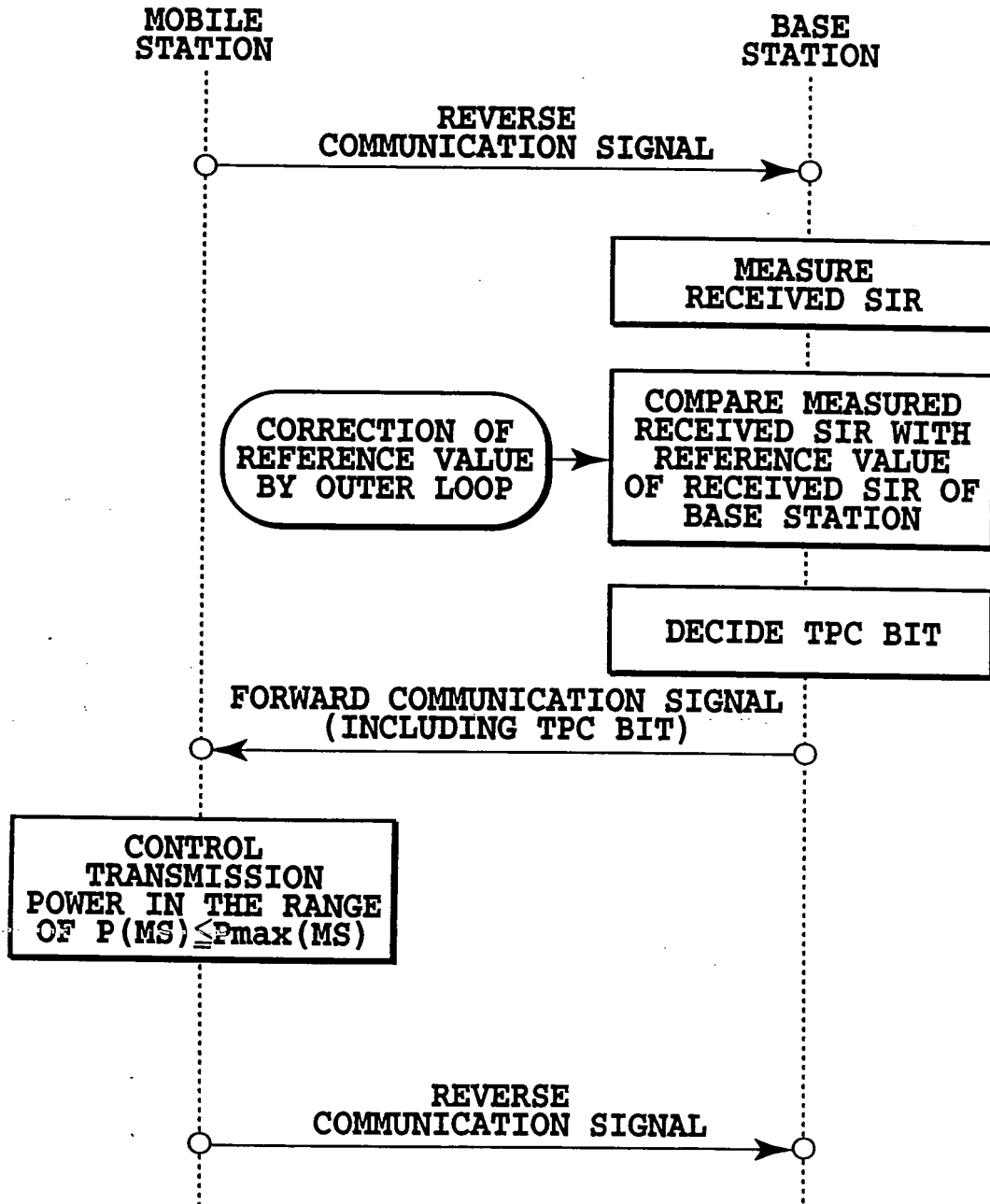


FIG.40

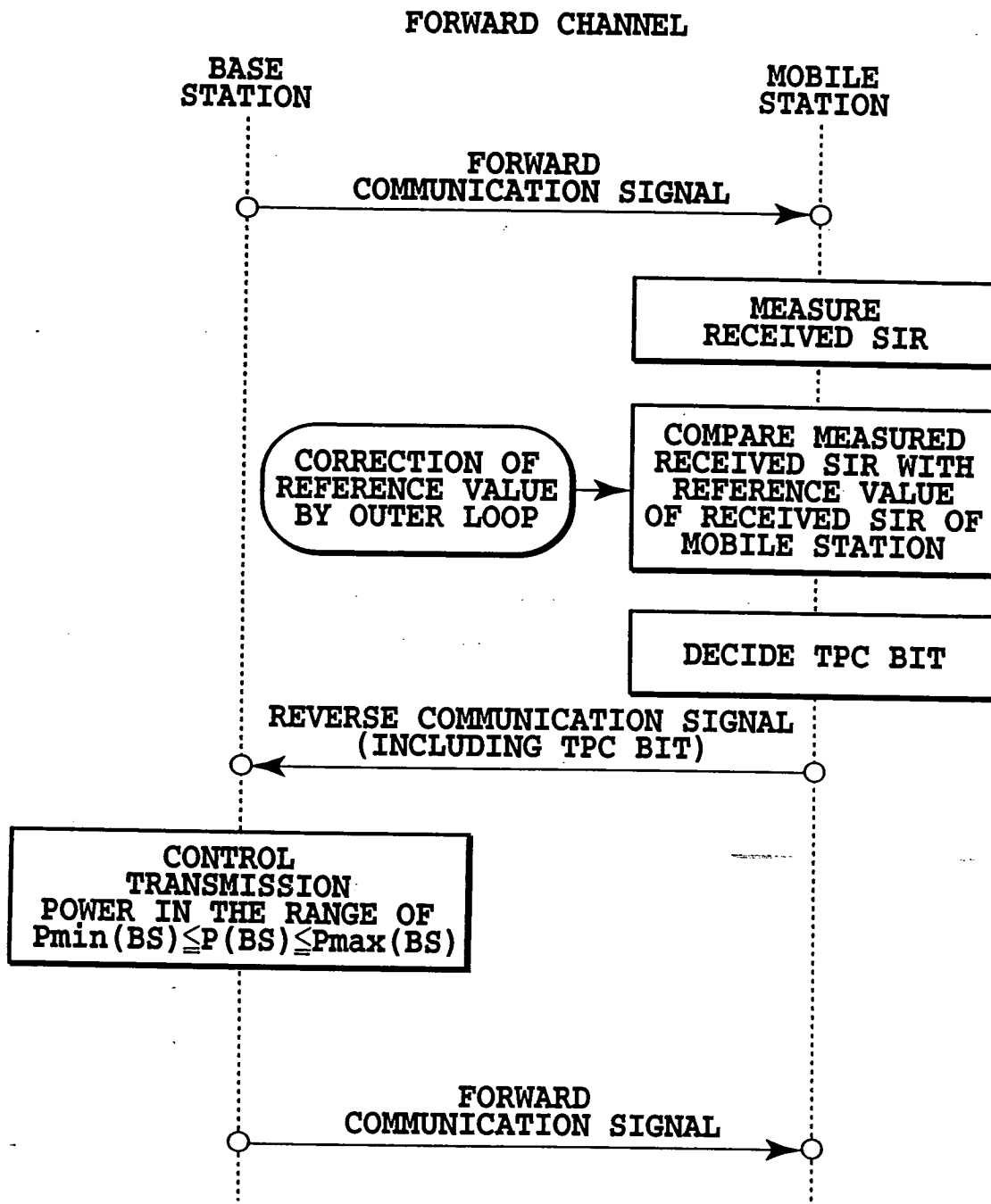
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REVERSE CHANNEL



$P(MS)$ • • • REVERSE TRANSMISSION POWER
 $P_{max}(MS)$ • • • MAXIMUM REVERSE TRANSMISSION POWER
 $P(BS)$ • • • FORWARD TRANSMISSION POWER
 $P_{max}(BS)$ • • • MAXIMUM FORWARD TRANSMISSION POWER
 $P_{min}(BS)$ • • • MINIMUM FORWARD TRANSMISSION POWER

FIG.41A

**FIG.41B**

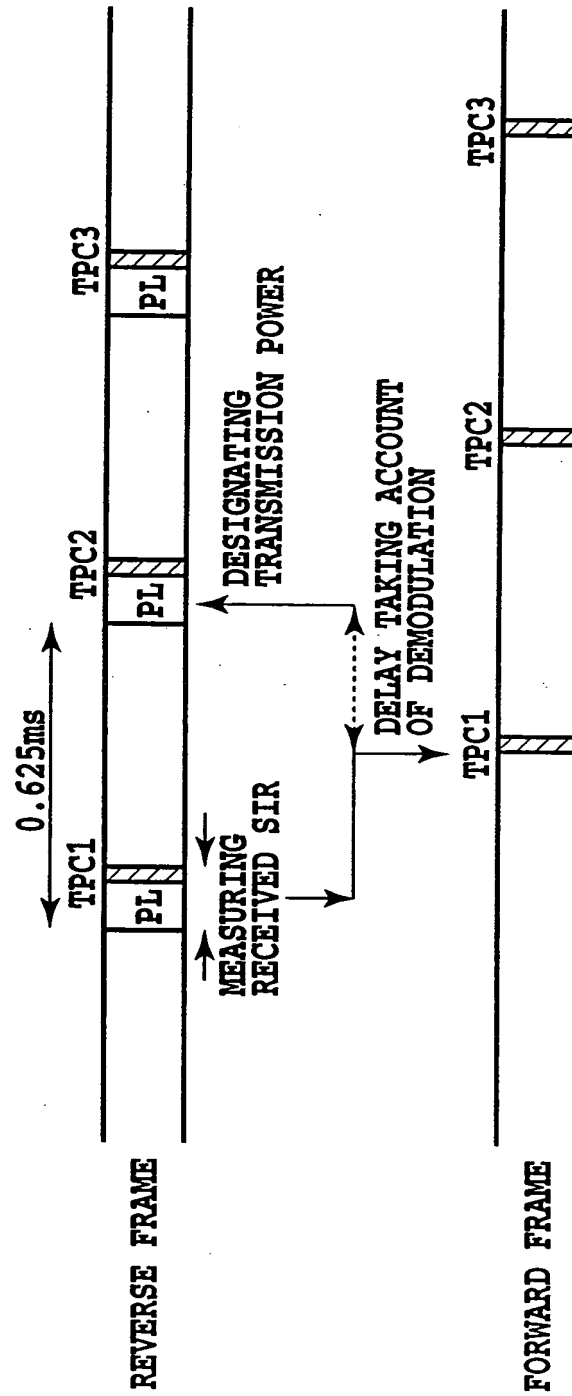
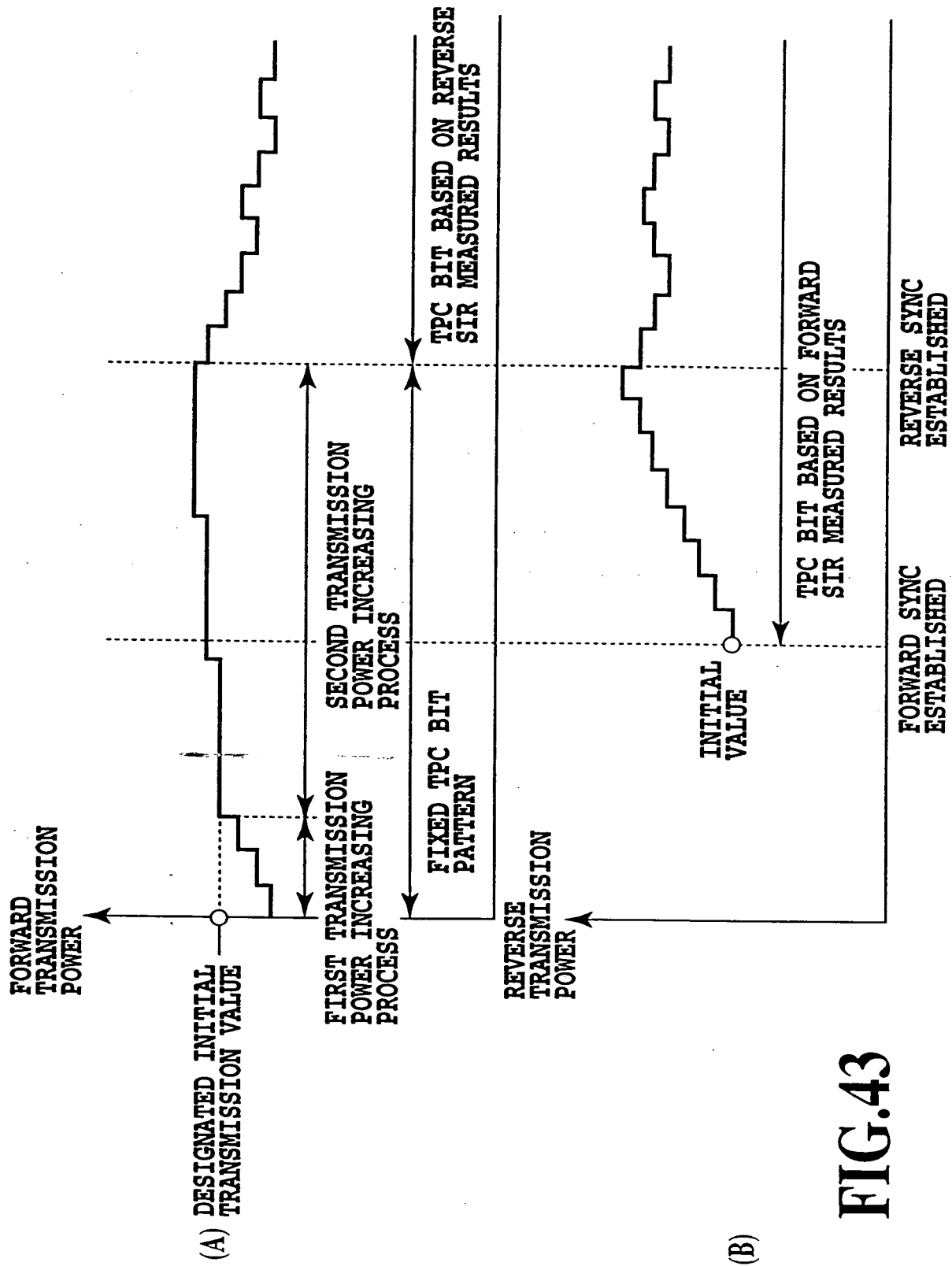


FIG.42



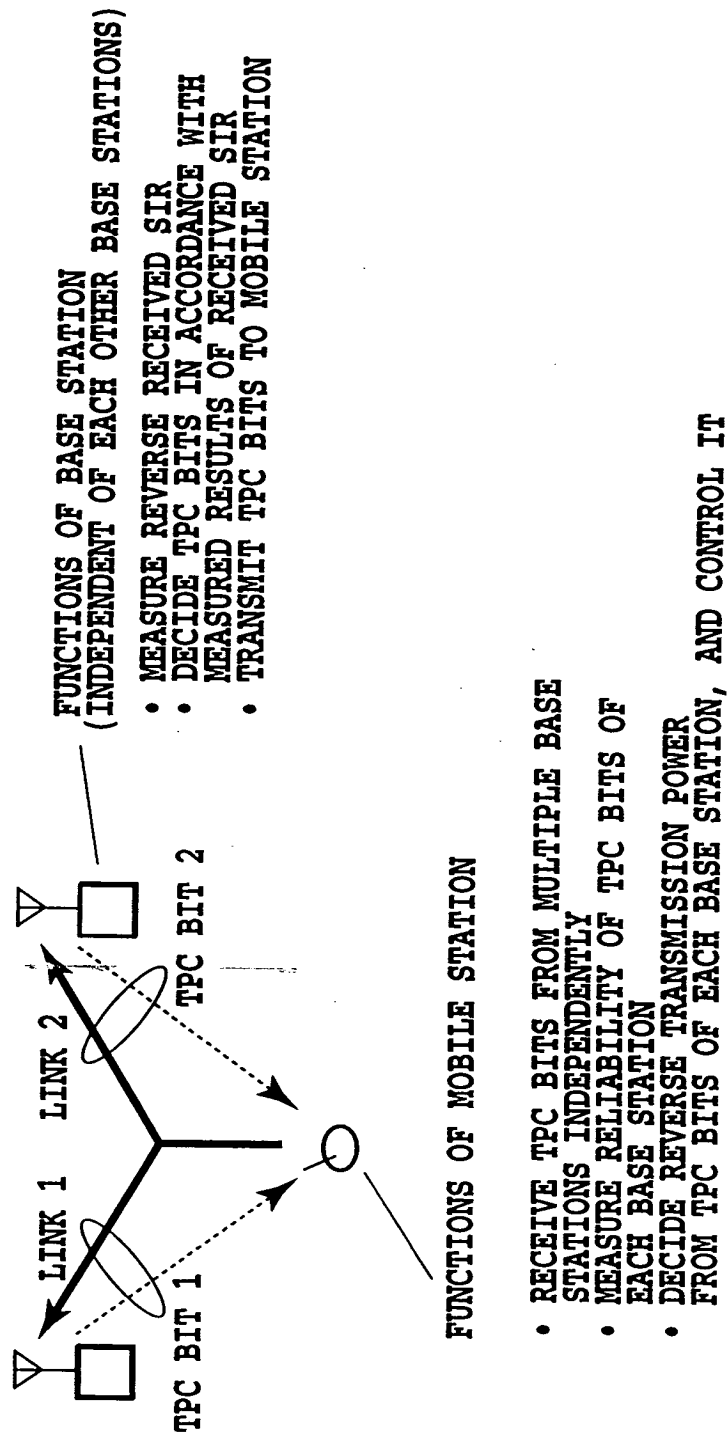


FIG.44

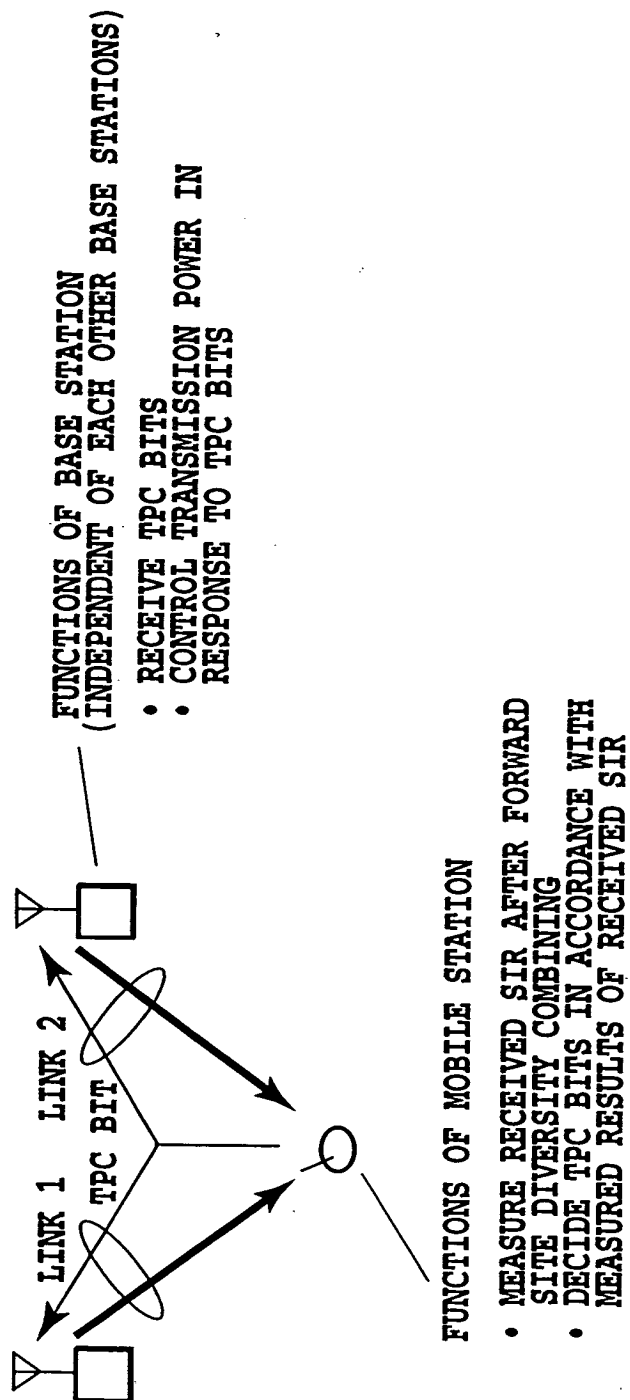


FIG.45

FIG.46

FIG.46A

FIG.46B

BASE STATION

START FORWARD DEDICATED CHANNEL TRANSMISSION

- INCREASE TRANSMISSION POWER GRADUALLY SO THAT OTHER USERS ARE UNAFFECTED (FIRST TRANSMISSION POWER INCREASING PROCESS)
- INFORMATION BITS CONSIST OF IDLE PATTERN (SEE, 4.1.10)
- TPC BITS ARE CONTROLLED IN ACCORDANCE WITH GRADUALLY INCREASING FIXED PATTERN

START REVERSE SYNC ESTABLISHMENT

CHIP SYNC ESTABLISHMENT

DECIDE FRAME ALIGNMENT
(WITH DETECTING SW)

REVERSE SYNC IS ESTABLISHED

DECIDE TPC BIT IN RESPONSE TO MEASURED RESULT OF REVERSE SIR

MOBILE STATION

START FORWARD SYNC ESTABLISHMENT

CHIP SYNC ESTABLISHMENT

DECIDE FRAME ALIGNMENT
(WITH DETECTING SW)

FORWARD SYNC IS ESTABLISHED

START REVERSE DEDICATED CHANNEL TRANSMISSION

- INFORMATION BITS CONSIST OF IDLE PATTERN (SEE, 4.1.10)
- TRANSMISSION POWER IS DECIDED ACCORDING TO TPC BITS TRANSMITTED FROM BASE STATION
- TPC BITS ARE DECIDED IN ACCORDANCE WITH MEASURED RESULTS OF FORWARD SIR

FIG.46A

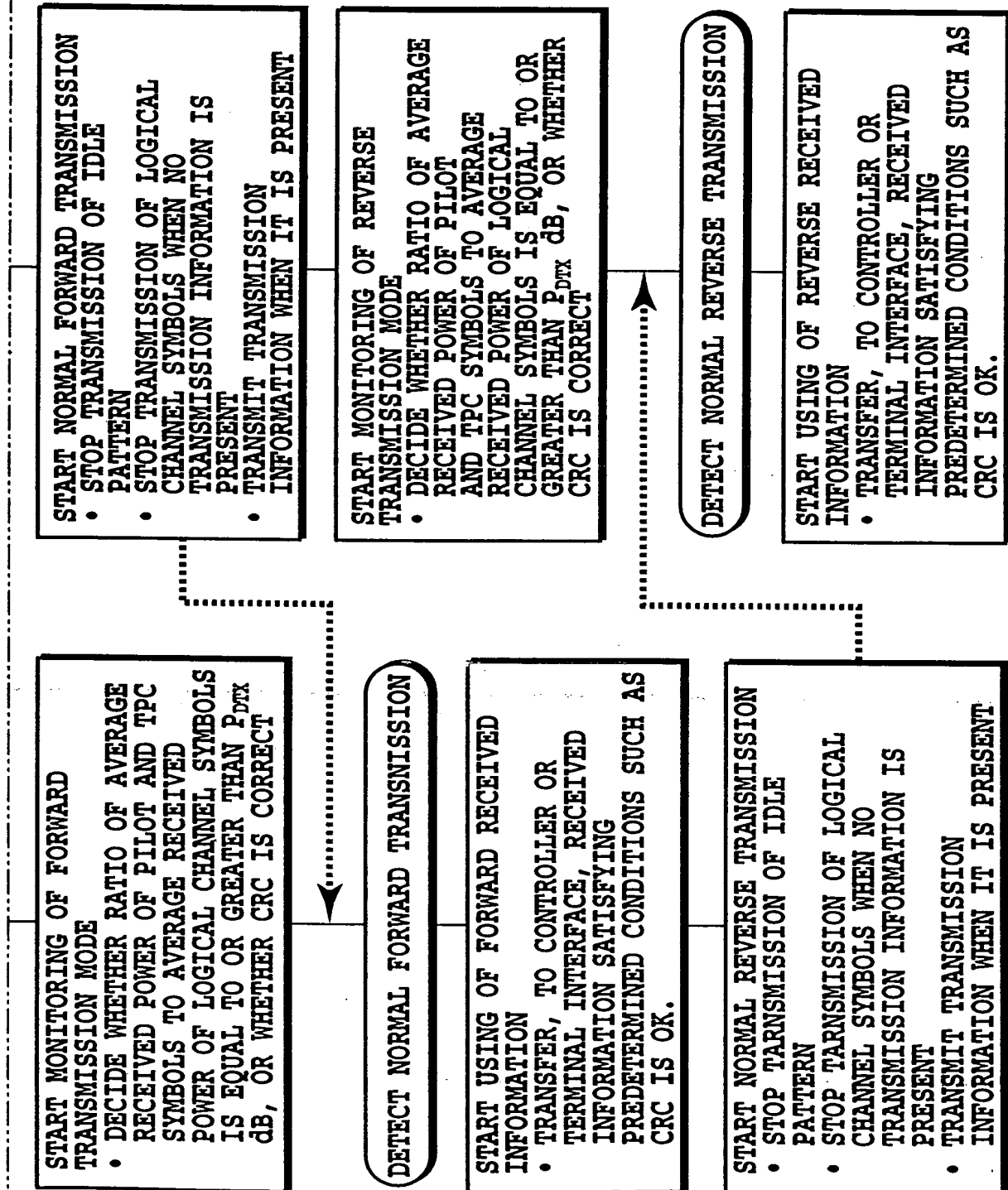


FIG. 46B

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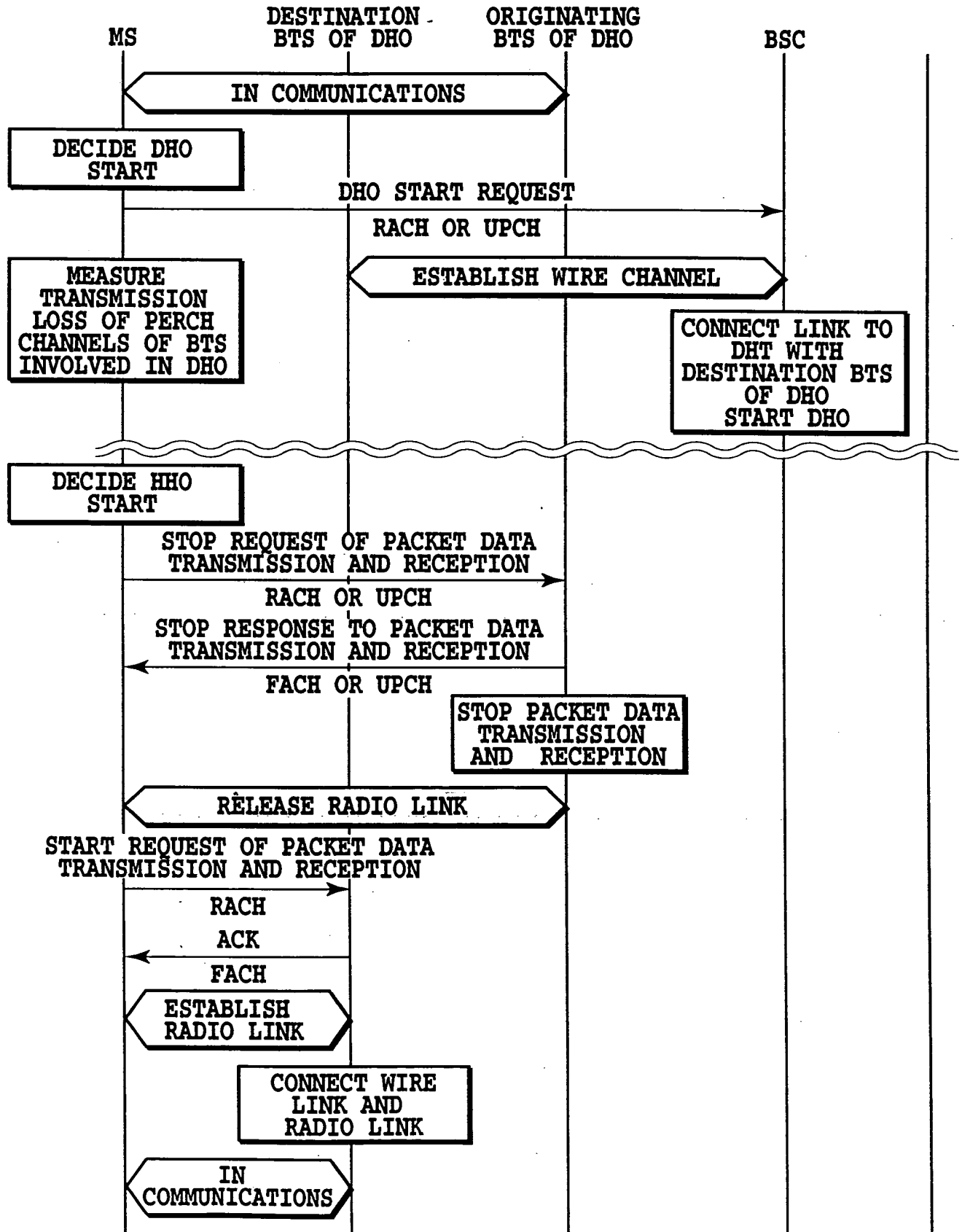
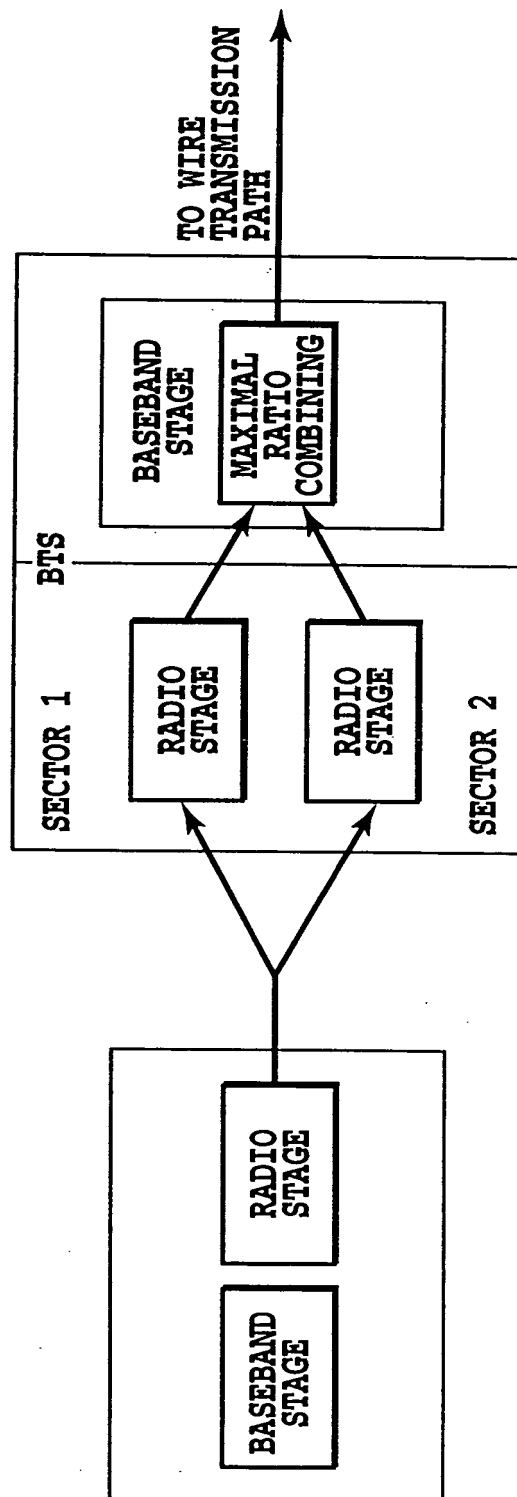
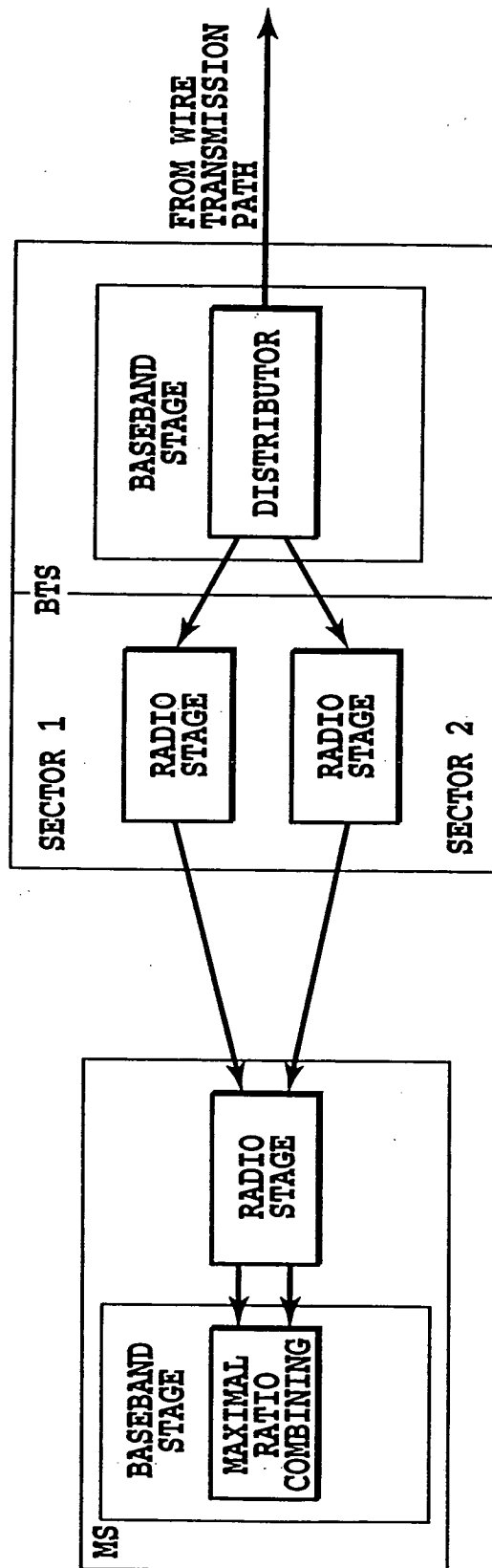


FIG.47



REVERSE DEDICATED PHYSICAL CHANNEL (UPCH)

FIG.48



FORWARD DEDICATED PHYSICAL CHANNEL (UPCH)

FIG.49

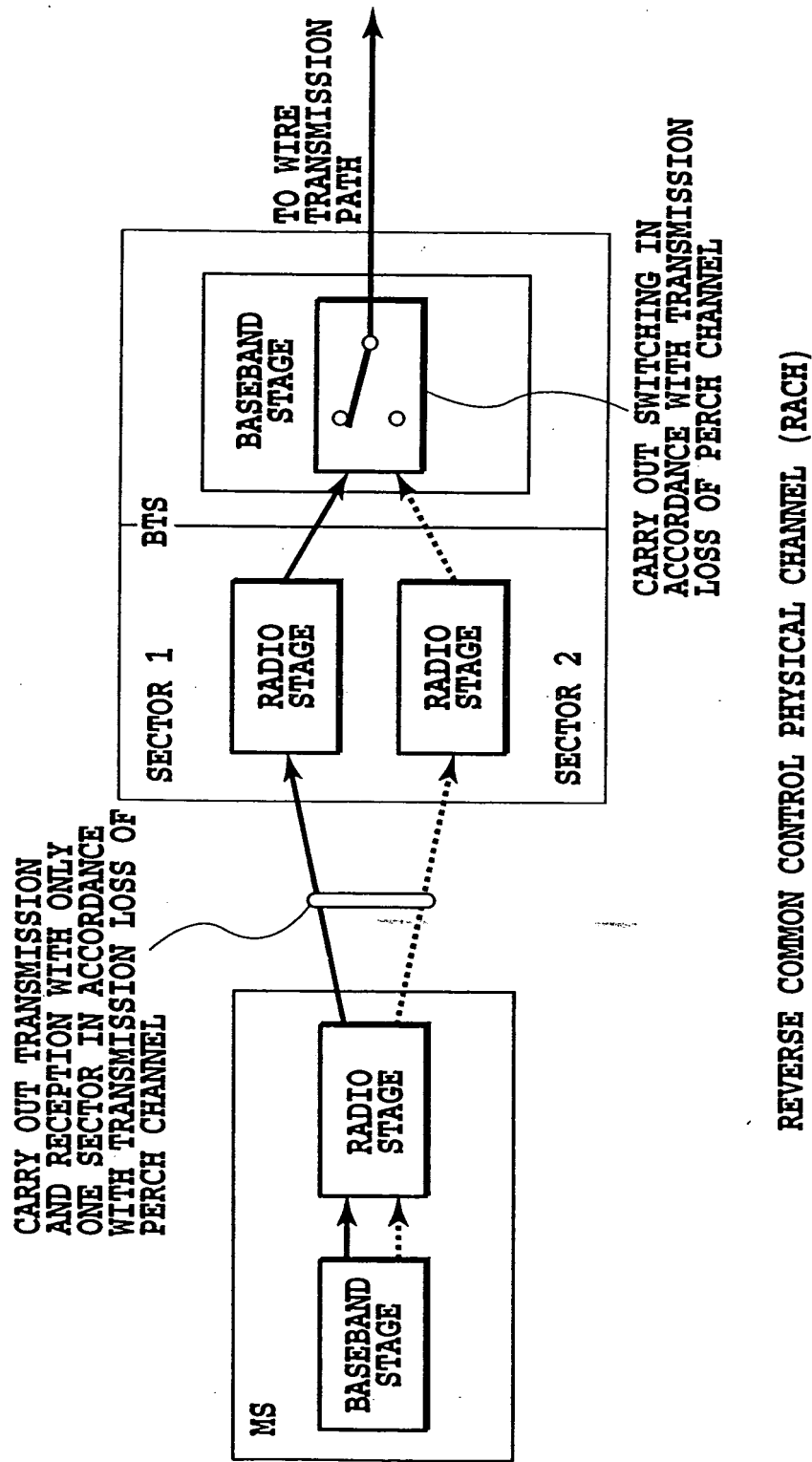


FIG.50

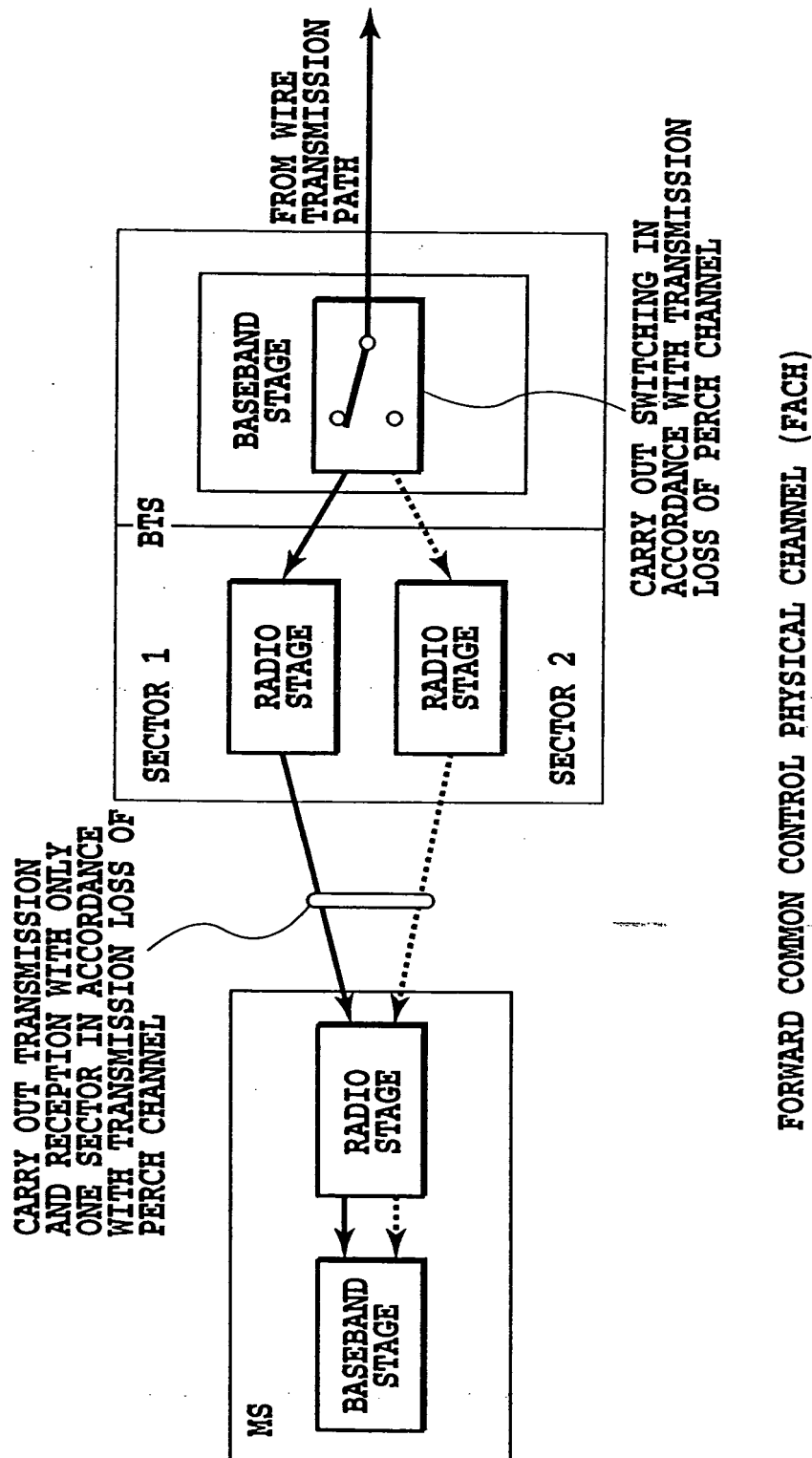
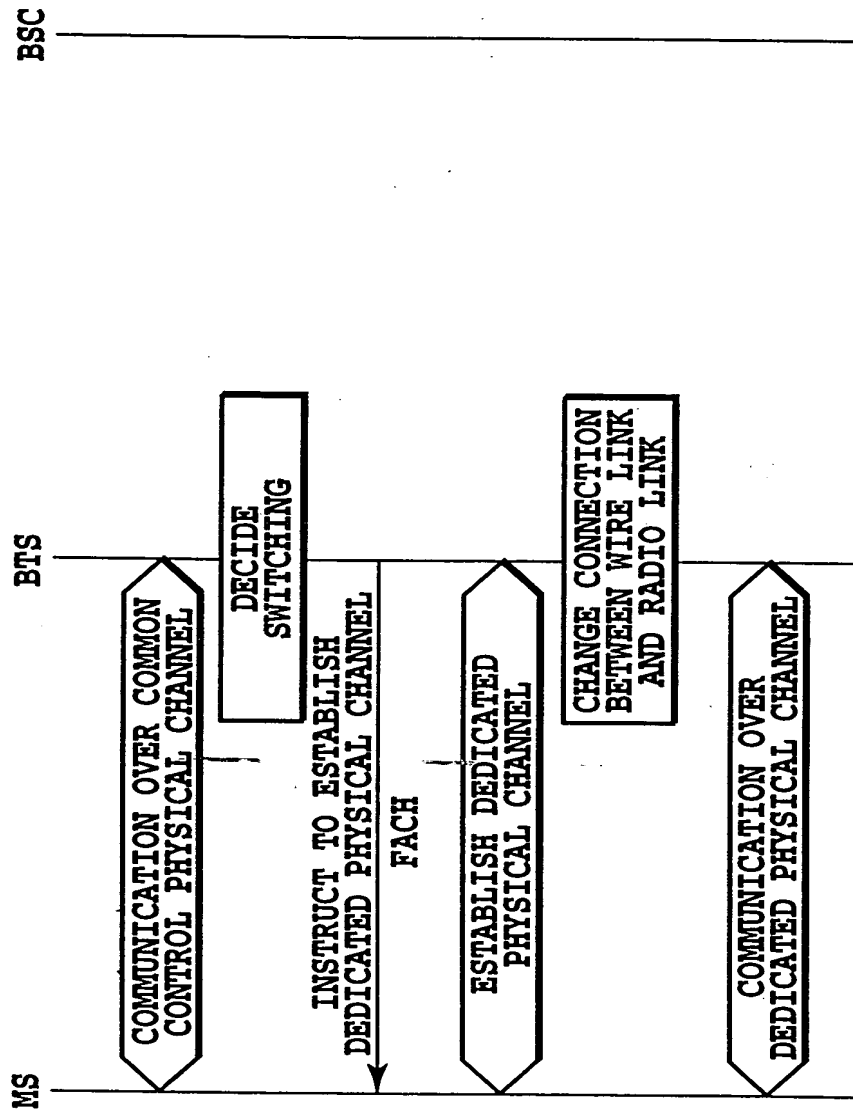


FIG.51



FROM COMMON CONTROL PHYSICAL CHANNEL
TO DEDICATED PHYSICAL CHANNEL

FIG.52

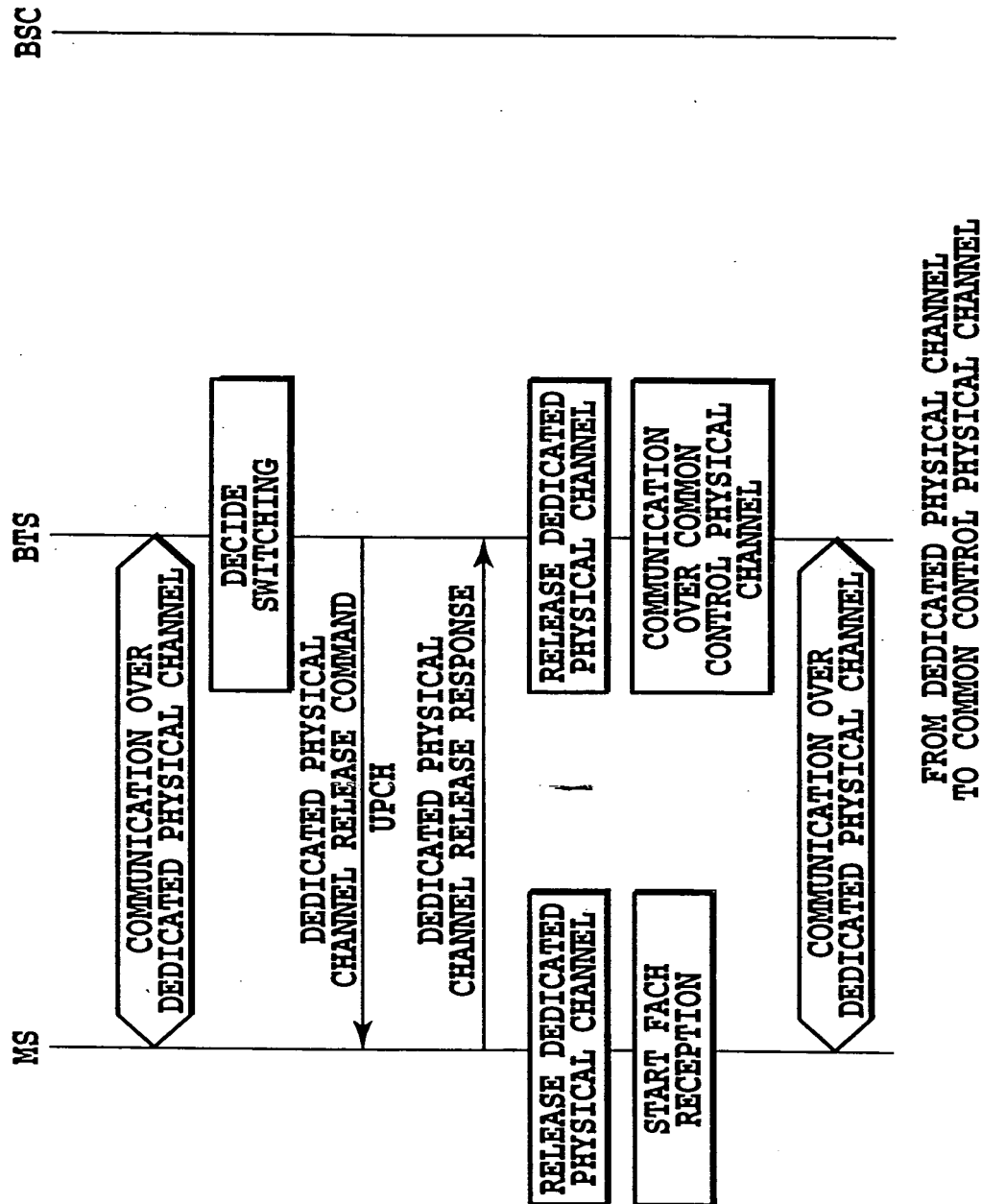


FIG.53

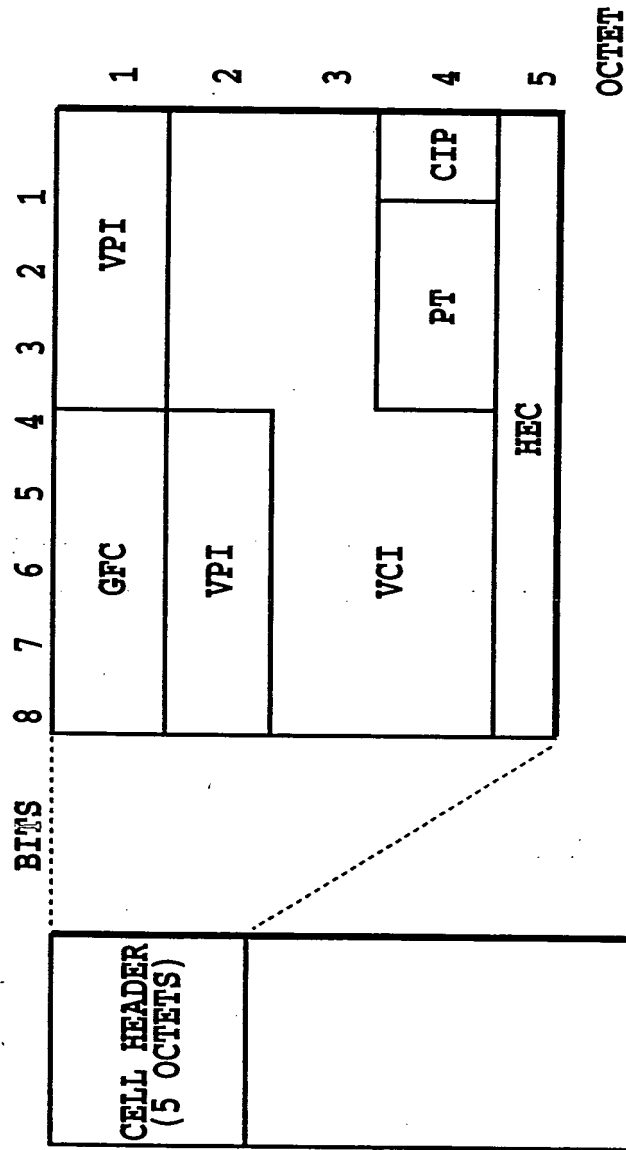


FIG.54

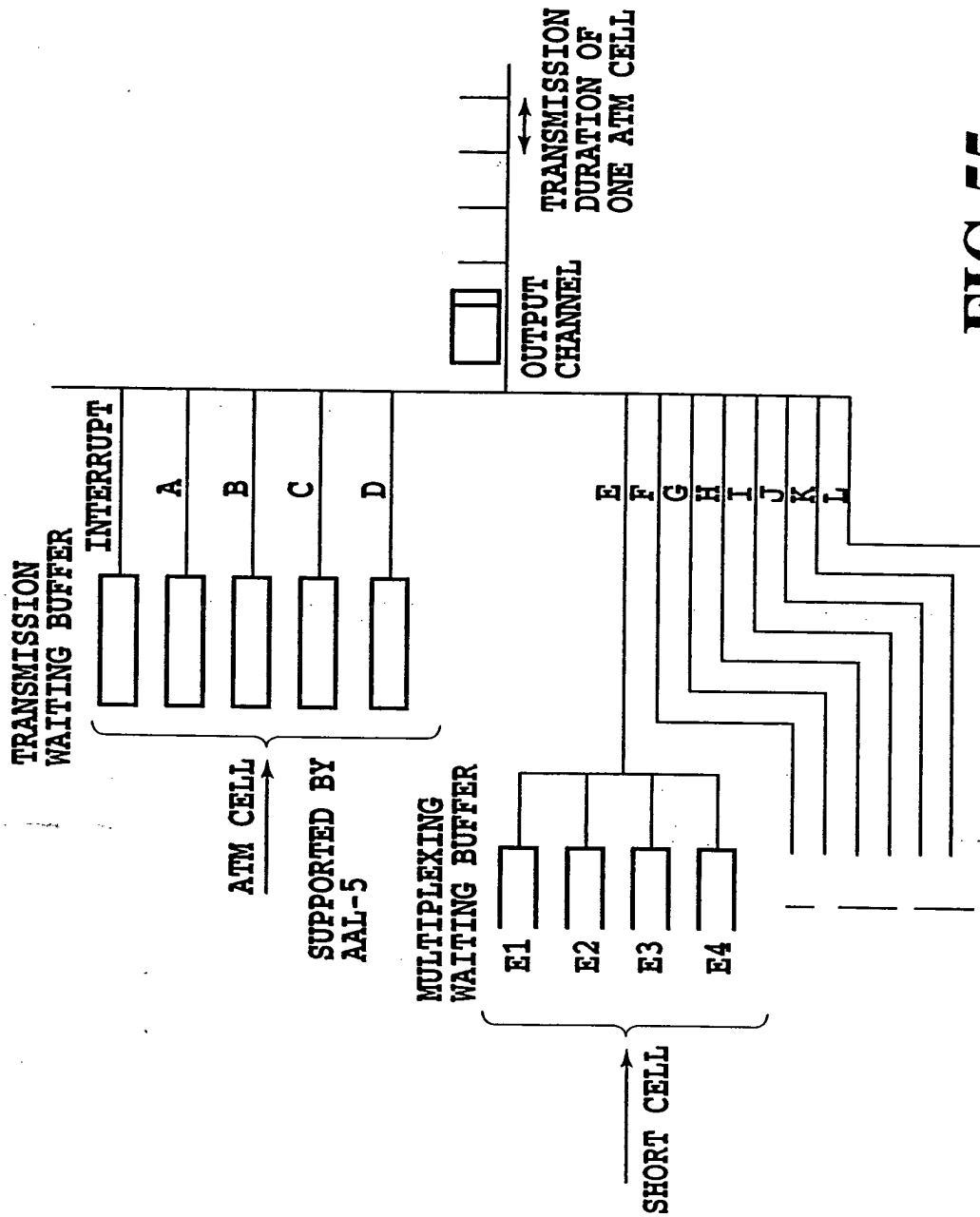


FIG.55

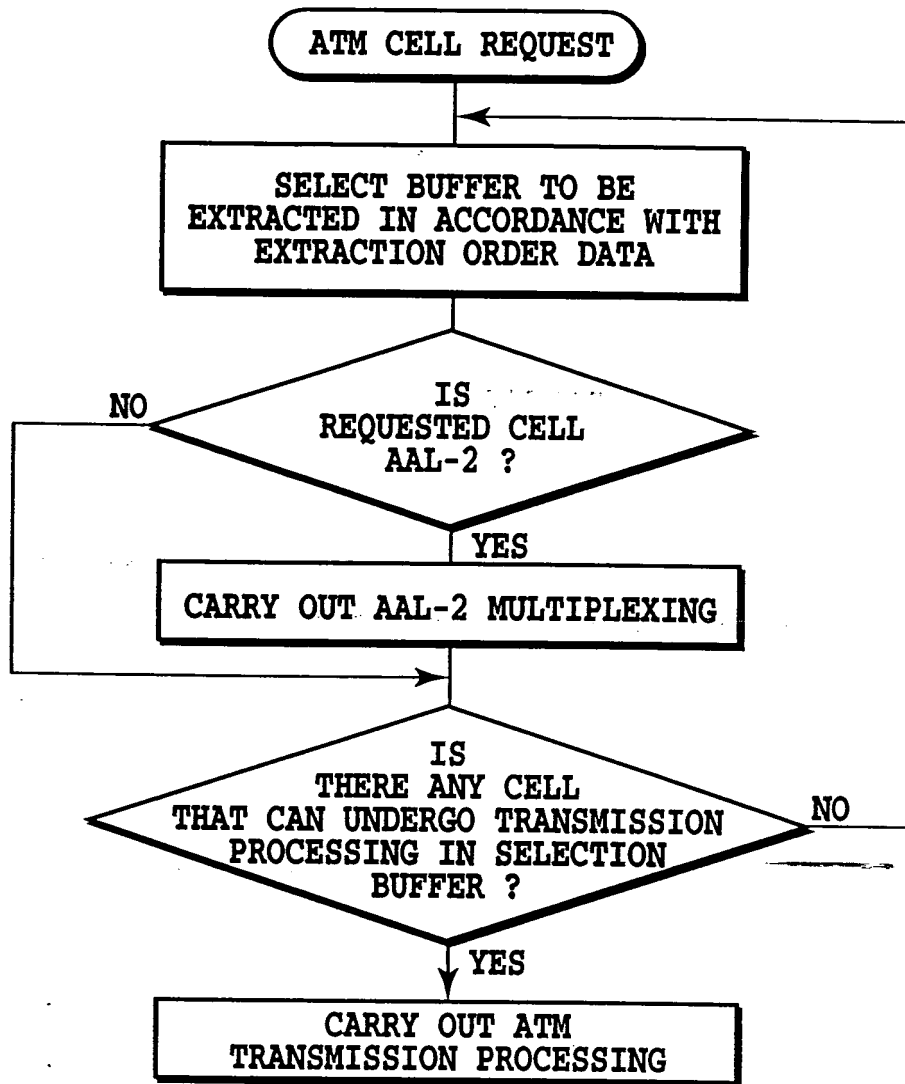


FIG.56

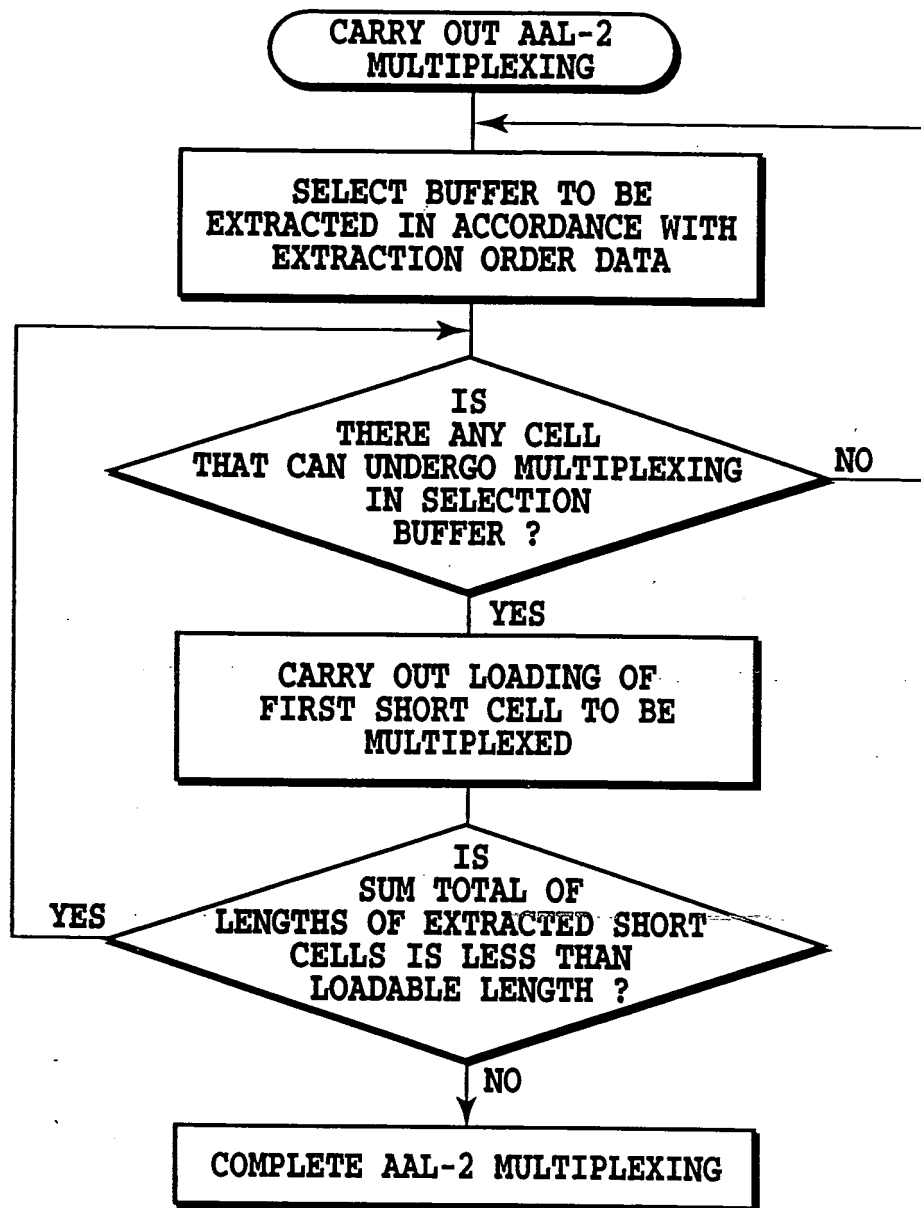


FIG.57

ATM CELL TRANSMISSION SEQUENCE TABLE
TRANSMISSION ORDER (ABOUT 256 AT MAXIMUM)

PRIORITY ↓

E	F	A	E	F	B	E	F	C	E	. . .
F	A	B	F	A	C	F	A	D	F	. . .
A	B	C	A	B	D	A	B	E	A	. . .
B	C	D	B	C	E	B	C	F	B	. . .
C	D	E	C	D	F	C	D	A	C	. . .
D	E	F	D	E	A	D	E	B	D	. . .

FIG.58A

SHORT CELL TRANSMISSION SEQUENCE TABLE
(QUALITY CLASS (6))
TRANSMISSION ORDER (ABOUT 128 AT MAXIMUM)

PRIORITY ↓

E1	E1	E1	E2	E1	E1	E1	E3	. . .
E2	E2	E2	E3	E2	E2	E2	E4	. . .
E3	E3	E3	E4	E3	E3	E3	E1	. . .
E4	E4	E4	E1	E4	E4	E4	E2	. . .

FIG.58B

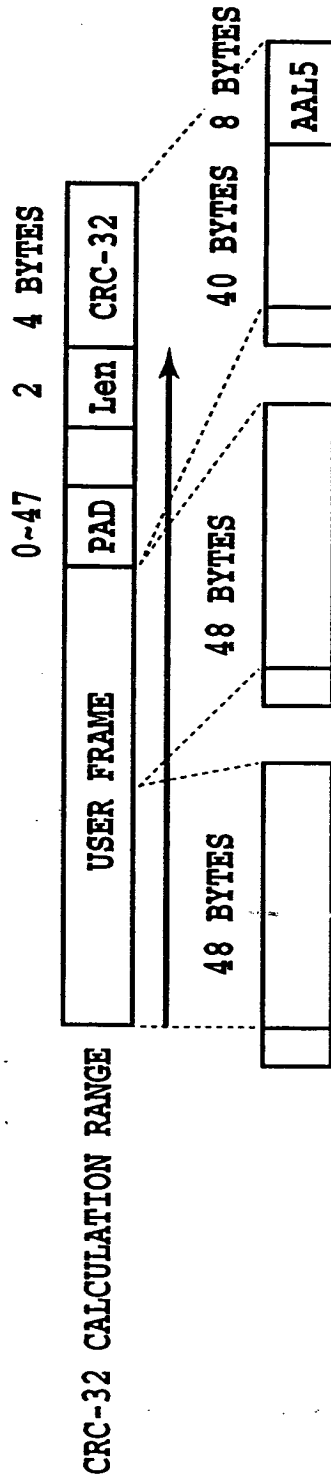
SHORT CELL TRANSMISSION SEQUENCE TABLE
(QUALITY CLASS (7))
TRANSMISSION ORDER (ABOUT 128 AT MAXIMUM)

PRIORITY ↓

F1	F1	F2	F1	F1	F3	F1	F1	. . .
F2	F2	F3	F2	F2	F4	F2	F2	. . .
F3	F3	F4	F3	F3	F1	F3	F3	. . .
F4	F4	F1	F4	F4	F2	F4	F4	. . .

FIG.58C

- CARRY OUT CELL EXTRACTION PROCESSING IN ACCORDANCE WITH TRANSMISSION SEQUENCE DETERMINED FOR EACH OUTPUT TIMING.
- IF NO CELL IS PRESENT IN HIGHER PRIORITY QUALITY CLASS, A CELL IN THE NEXT PRIORITY IS EXTRACTED.



PAD : PADDING BITS (ALL "0s")

Len : NUMBER OF BYTES OF EFFECTIVE DATA LENGTH OF USER FRAME

CRC-32 : CRC CHECKING BITS OVER 32 BITS

CRC-32 : GENERATOR POLYNOMIAL

$$G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$$

CHECK BITS ARE OBTAINED BY INVERTING BITS OF REMAINDER GENERATED BY THE GENERATOR POLYNOMIAL.

FIG.59

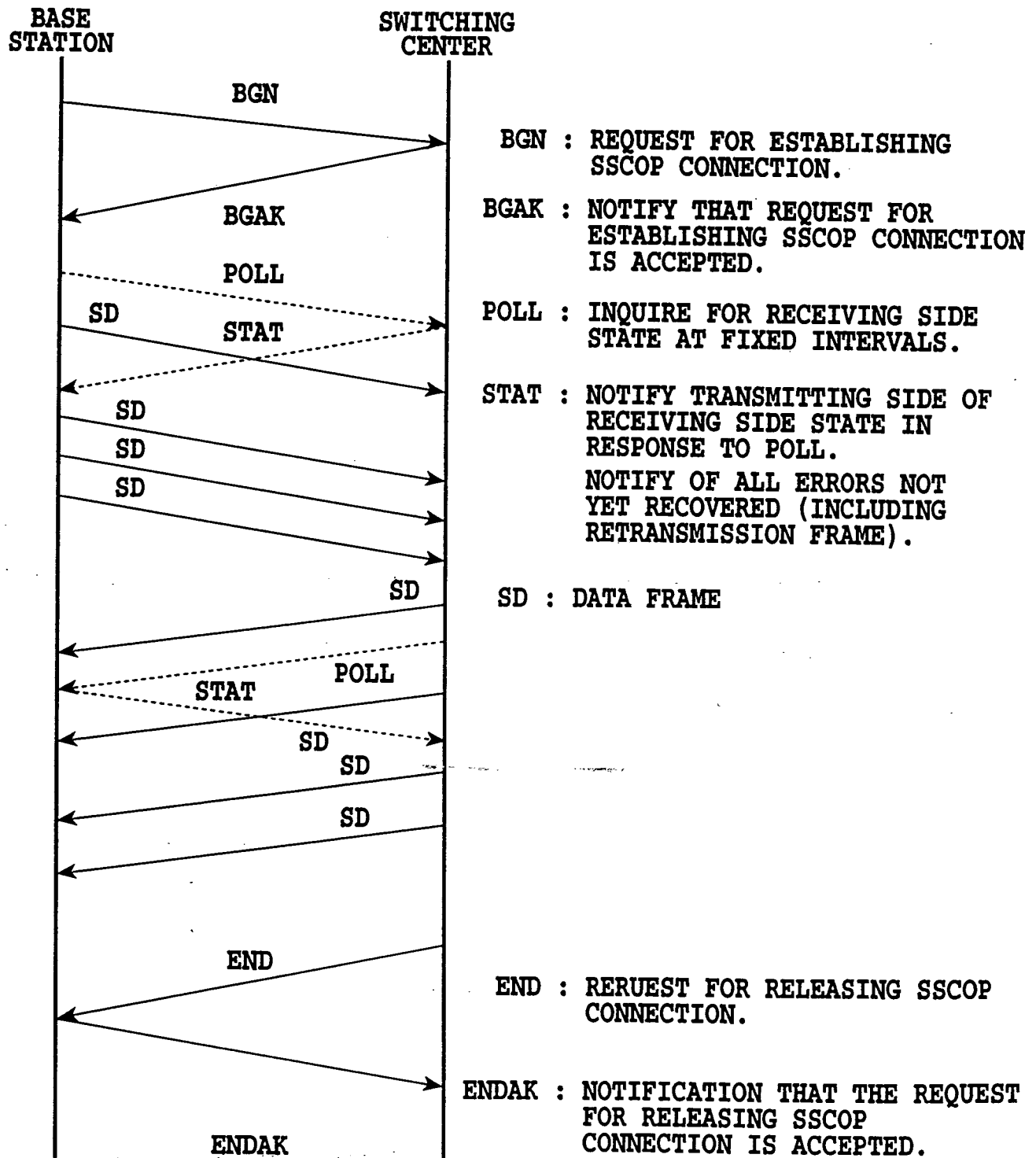


FIG.60

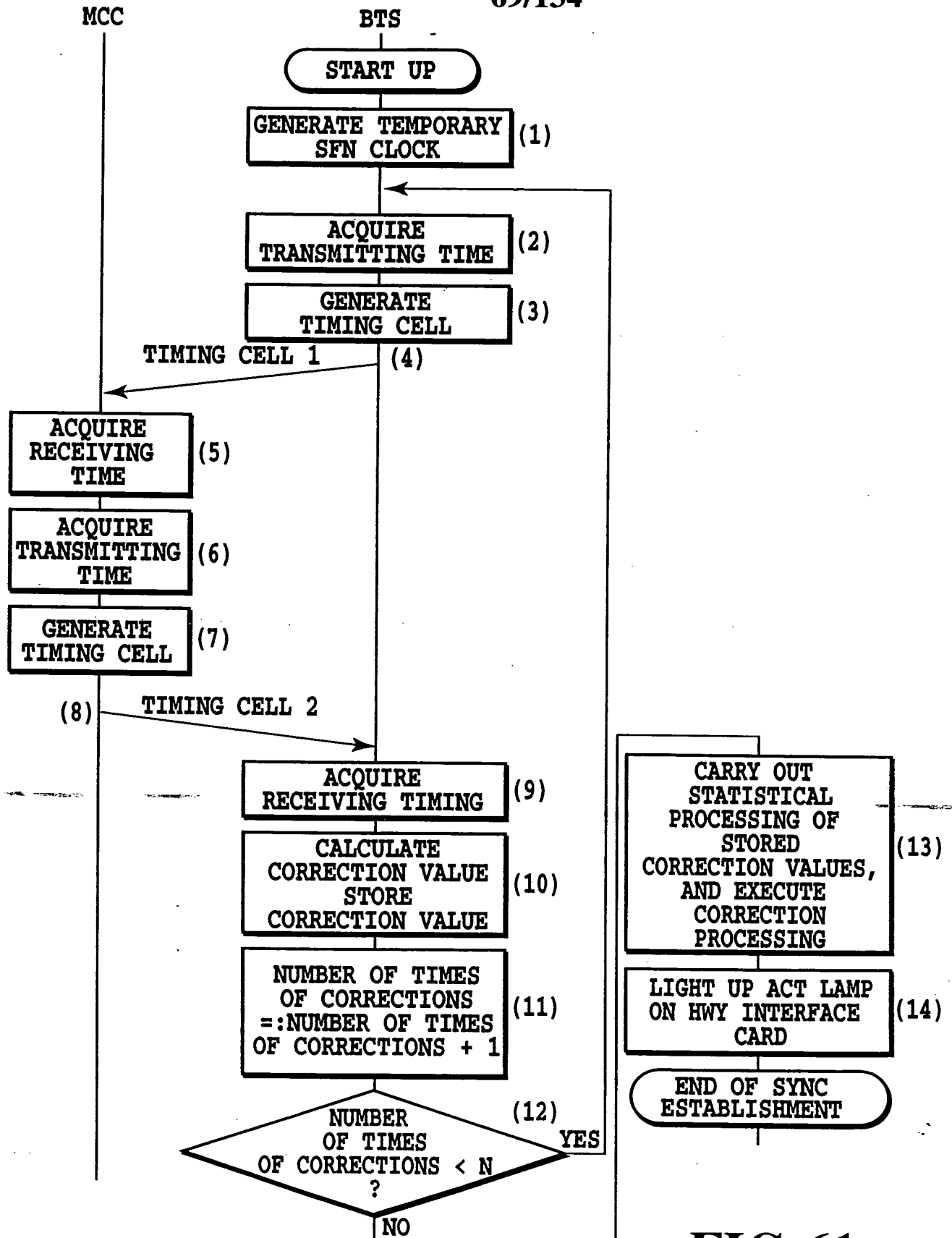
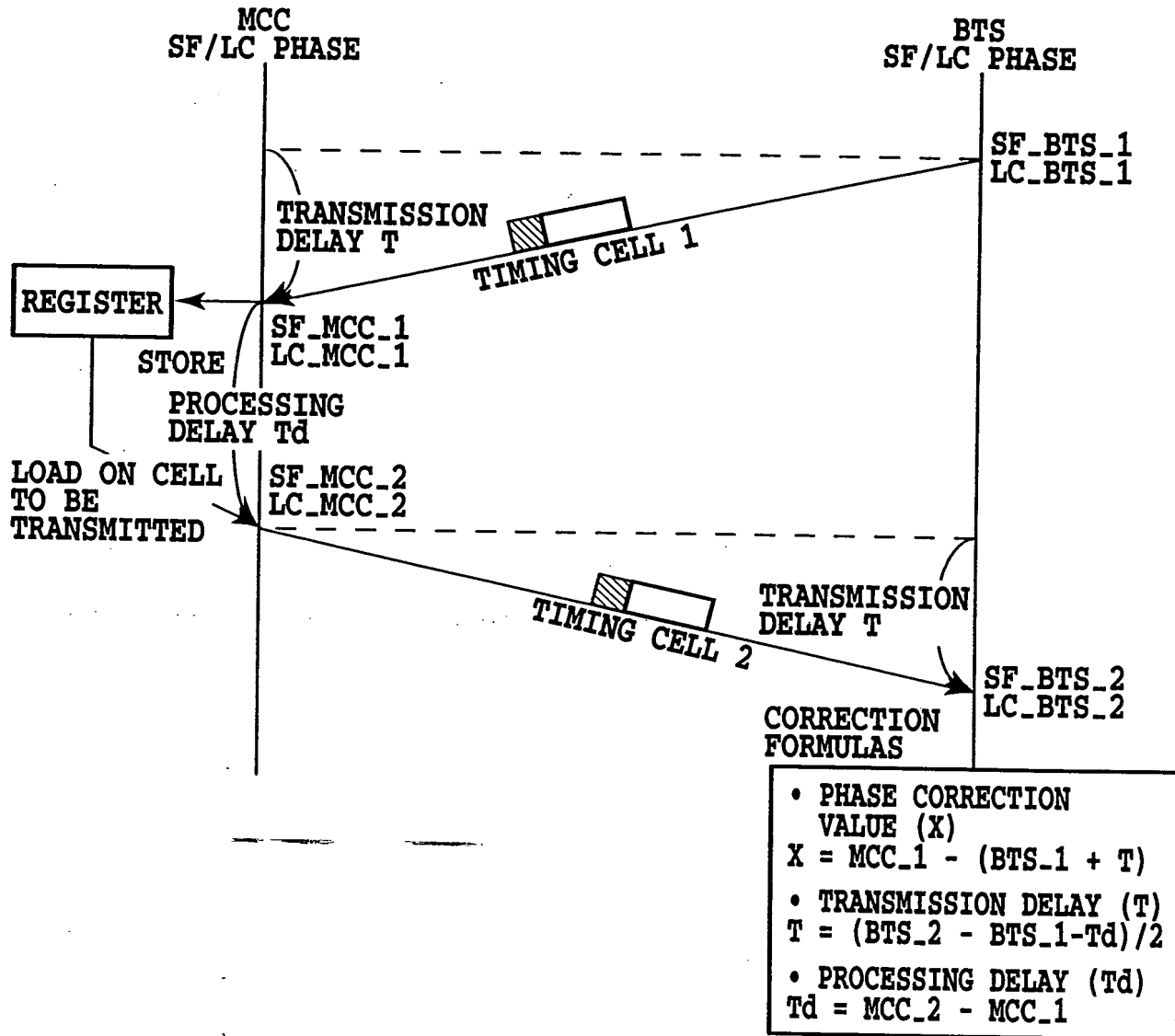


FIG.61



WHERE

$$MCC_1 = LC_MCC_1 \times 640(ms) + SF_MCC_1$$

$$MCC_2 = LC_MCC_2 \times 640(ms) + SF_MCC_2$$

$$BTS_1 = LC_BTS_1 \times 640(ms) + SF_BTS_1$$

$$BTS_2 = LC_BTS_2 \times 640(ms) + SF_BTS_2$$

FIG.62

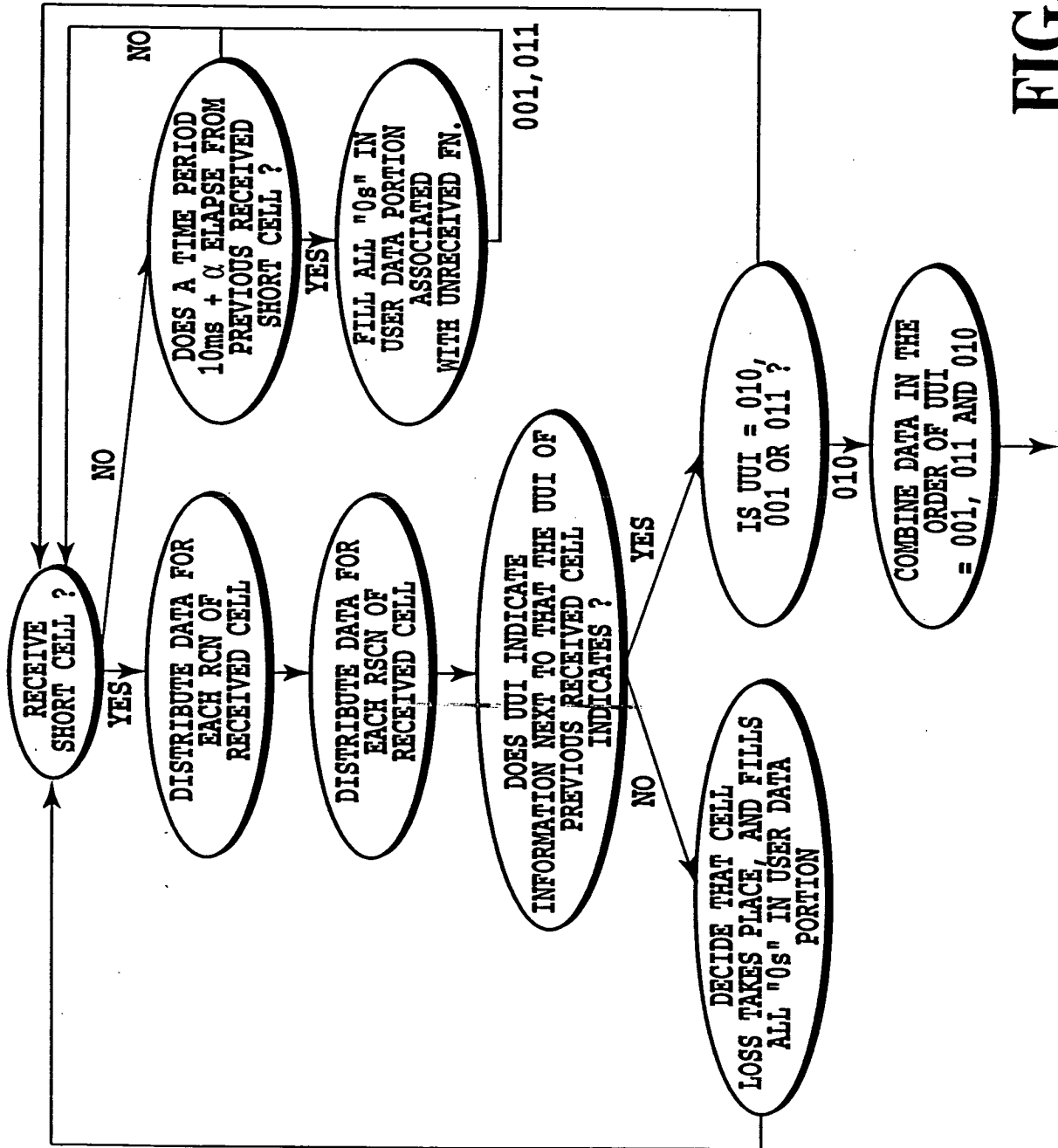


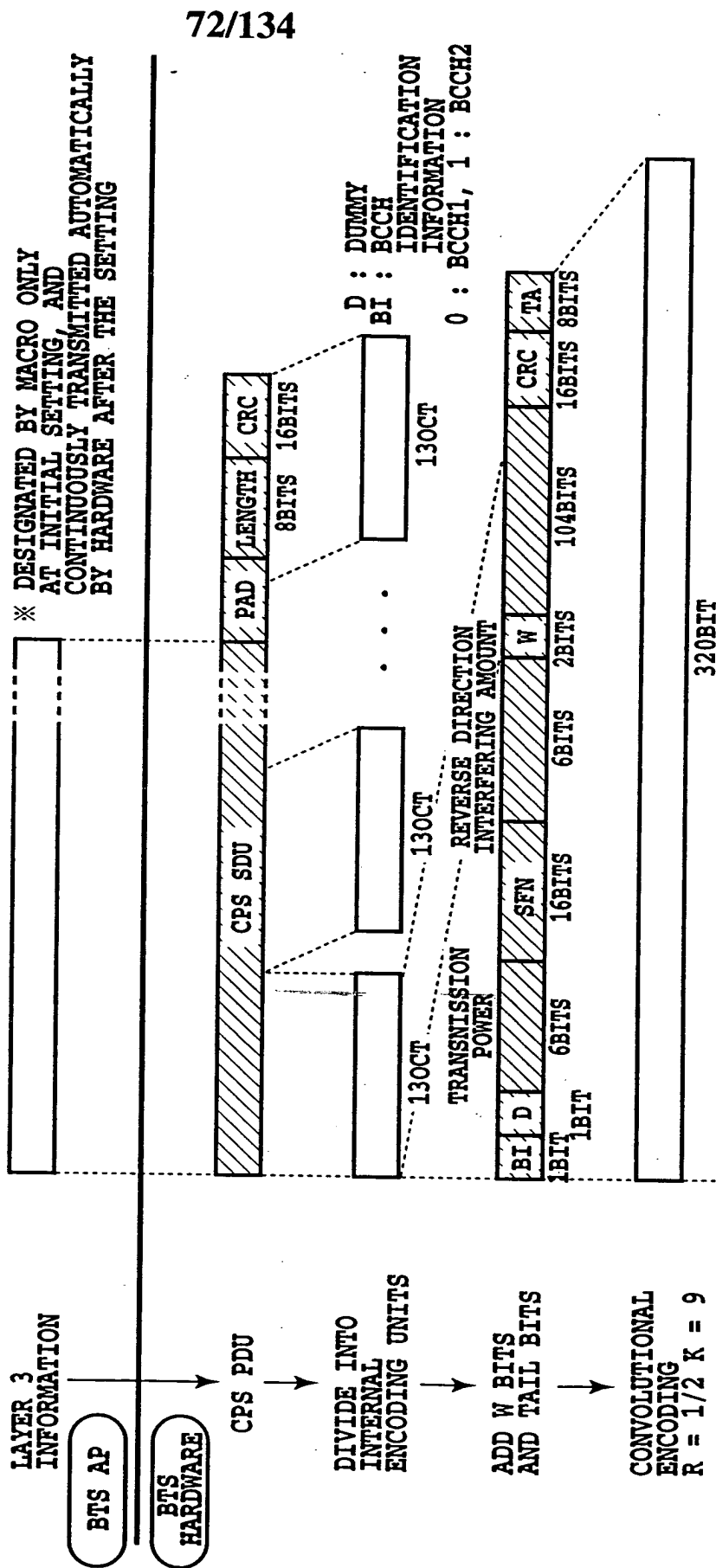
FIG. 63

FIG.64

FIG.64A

FIG.64B

FIG.64A



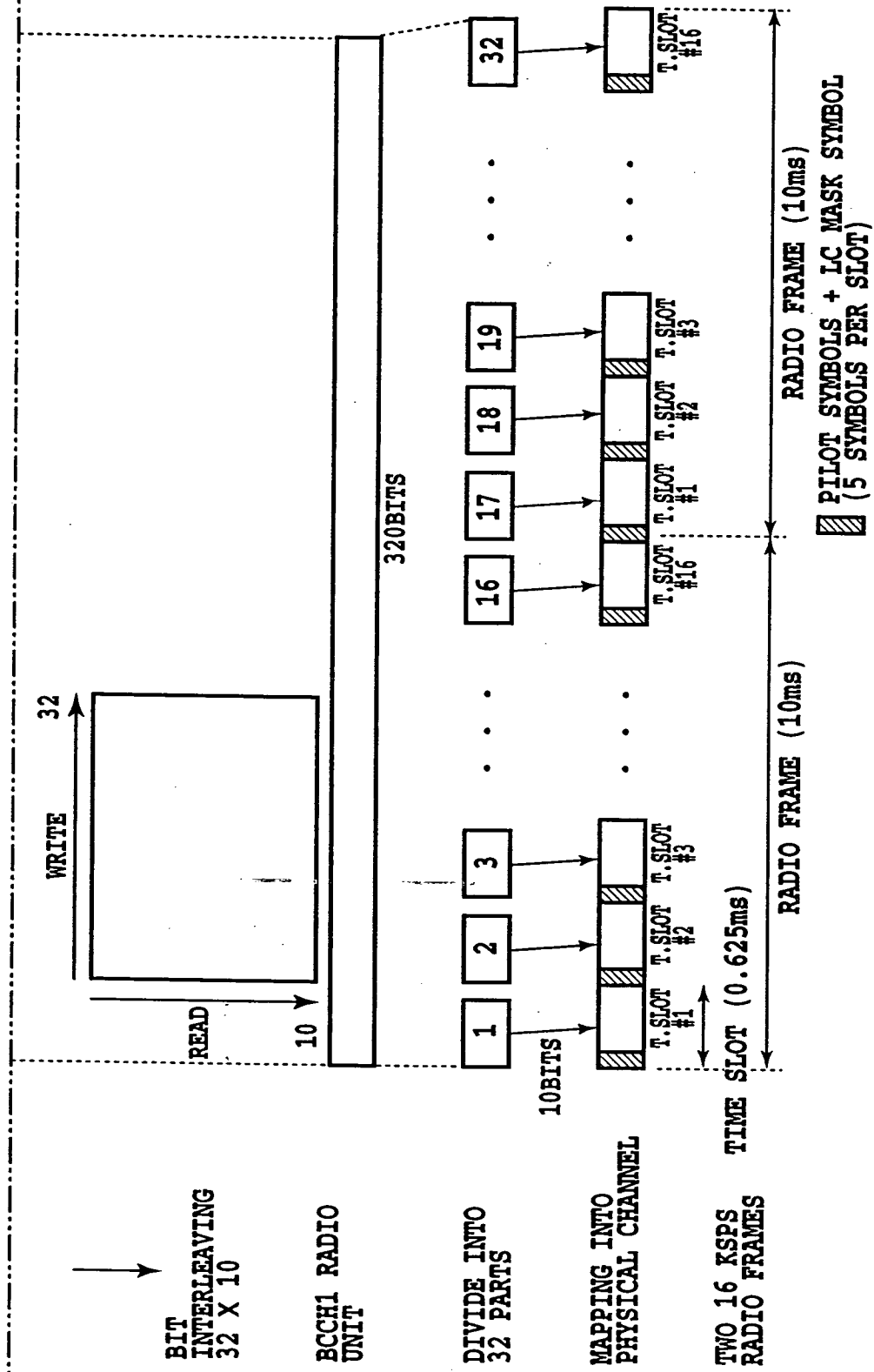


FIG.64B

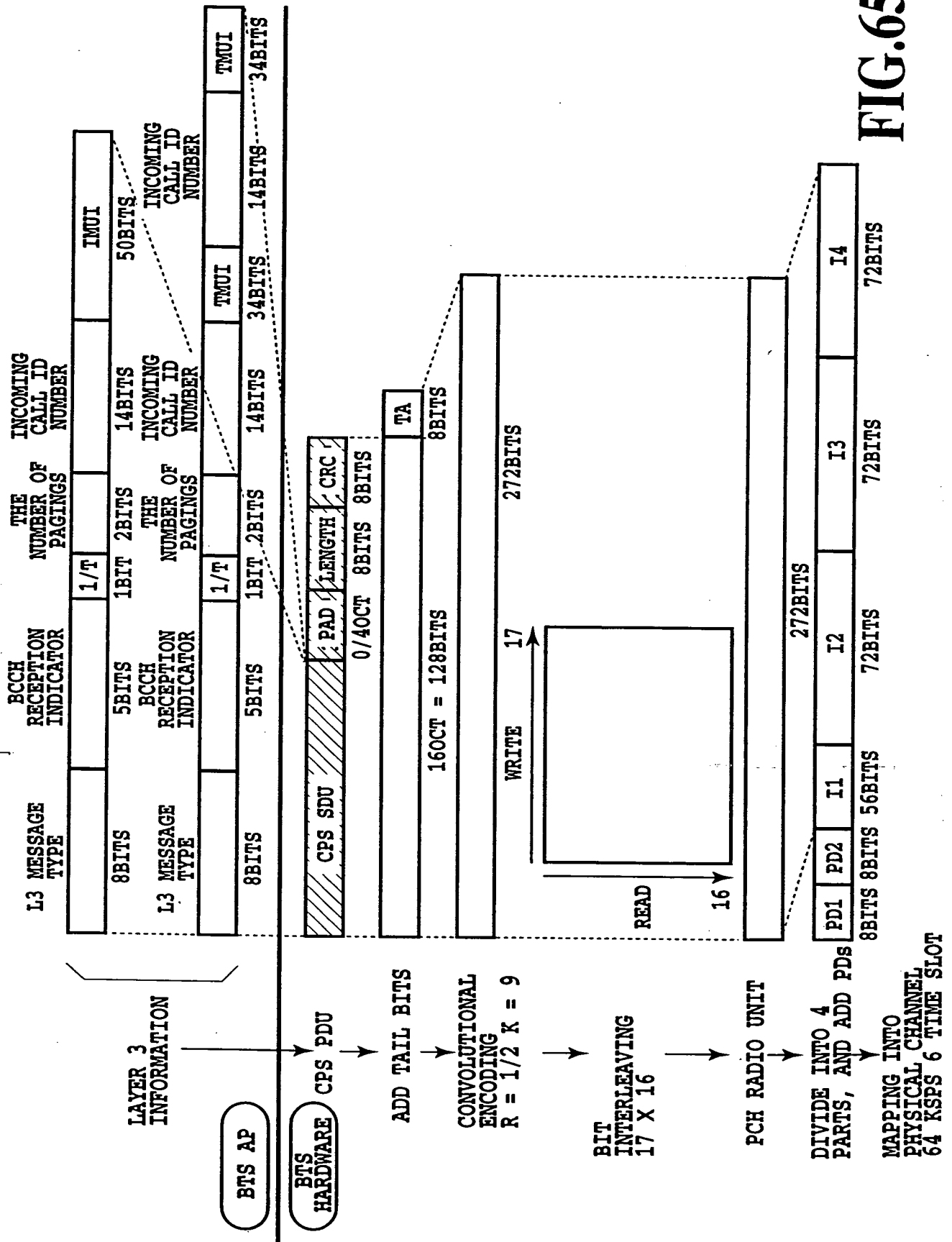


FIG.65A

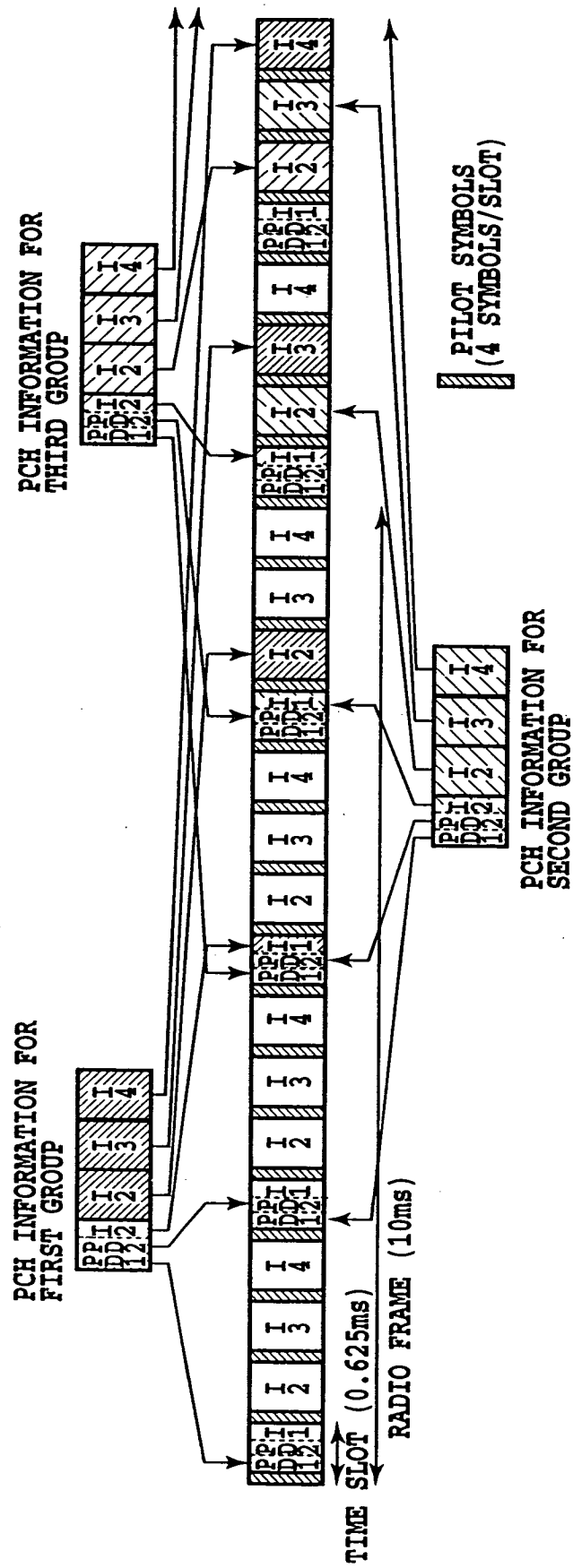


FIG.65B

FIG.66

FIG.66A

FIG.66B

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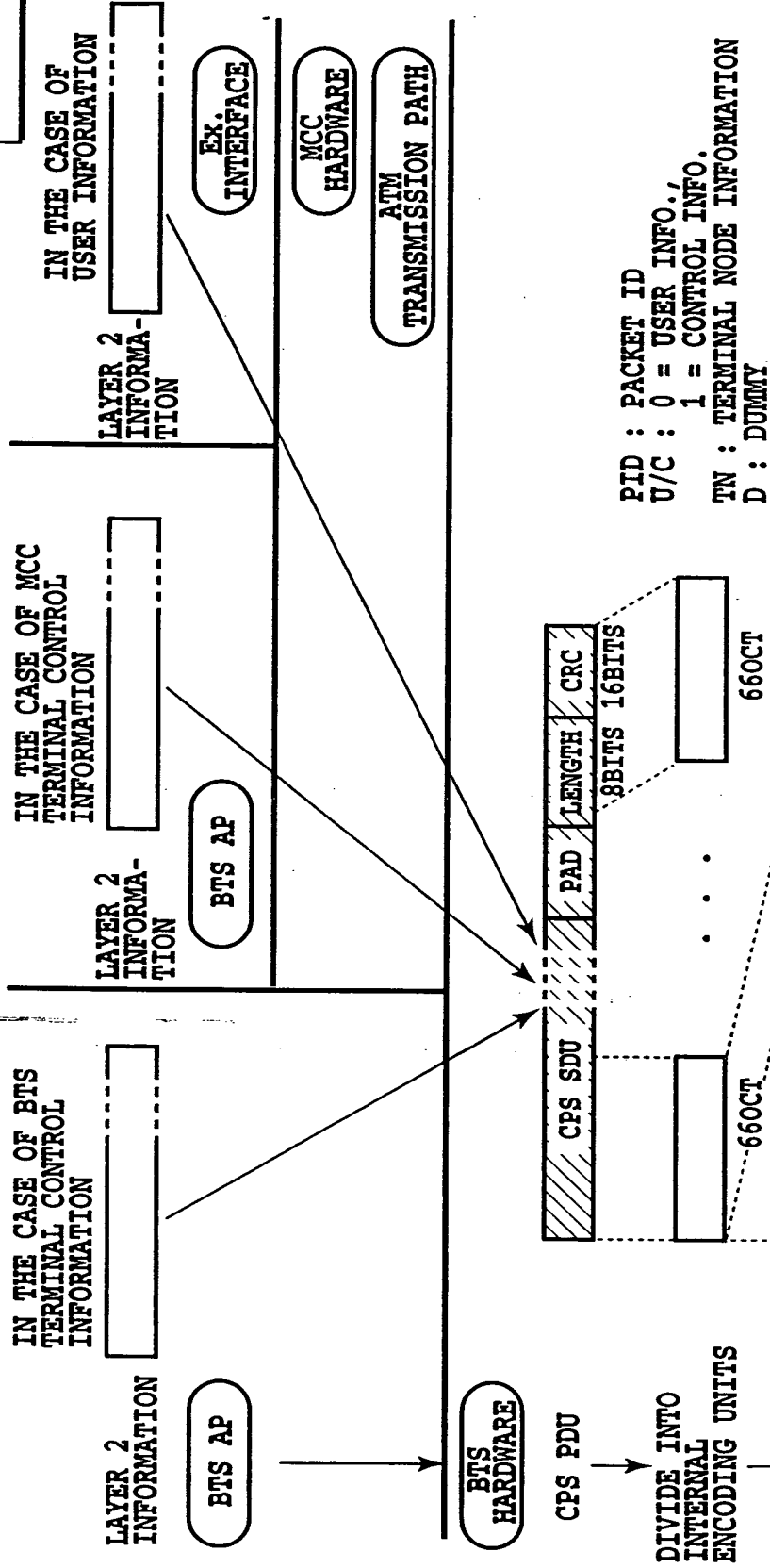


FIG.66A

Add PID, U/C, TN, W BITS, CRC BITS AND TAIL BITS

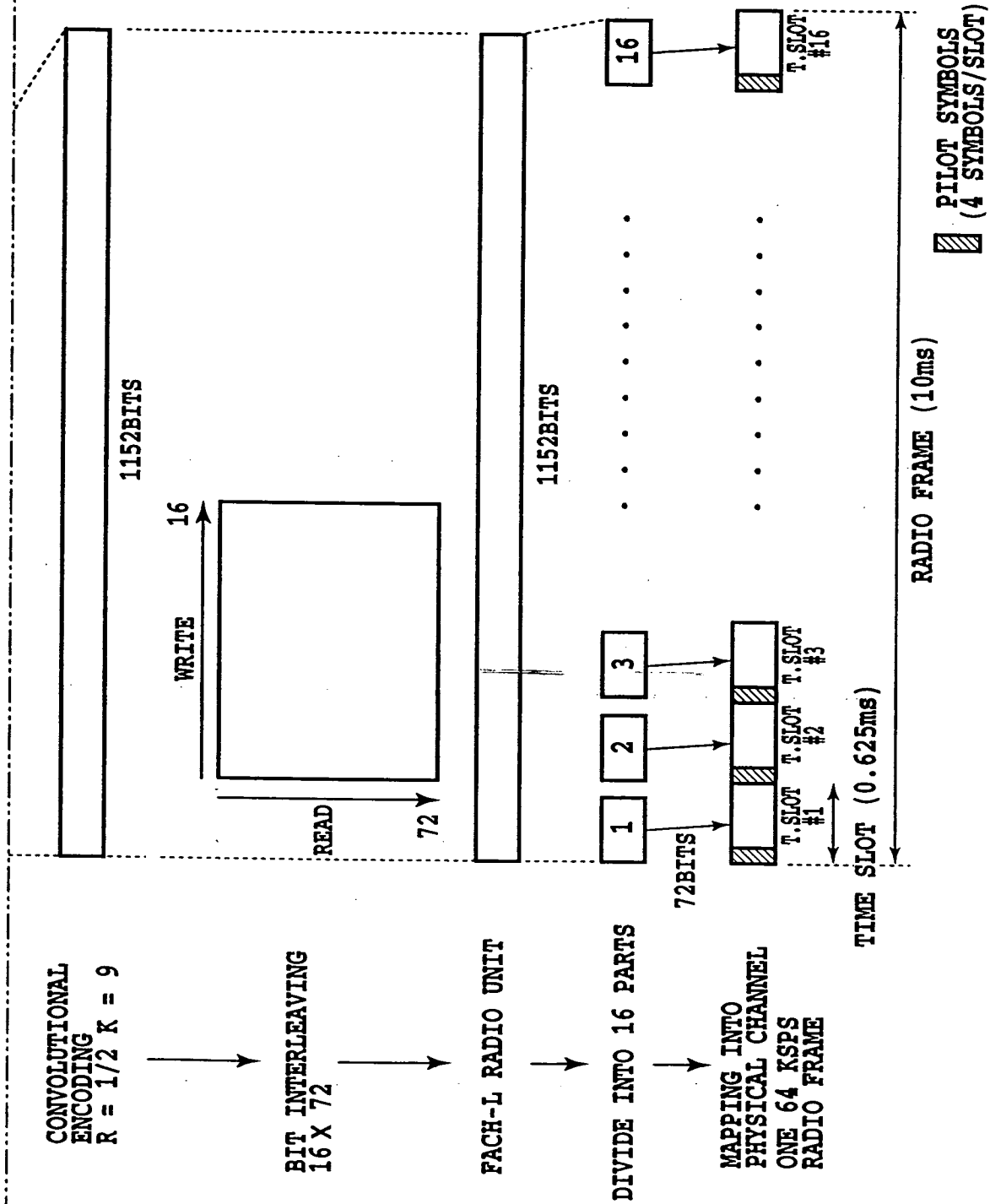


FIG.66B

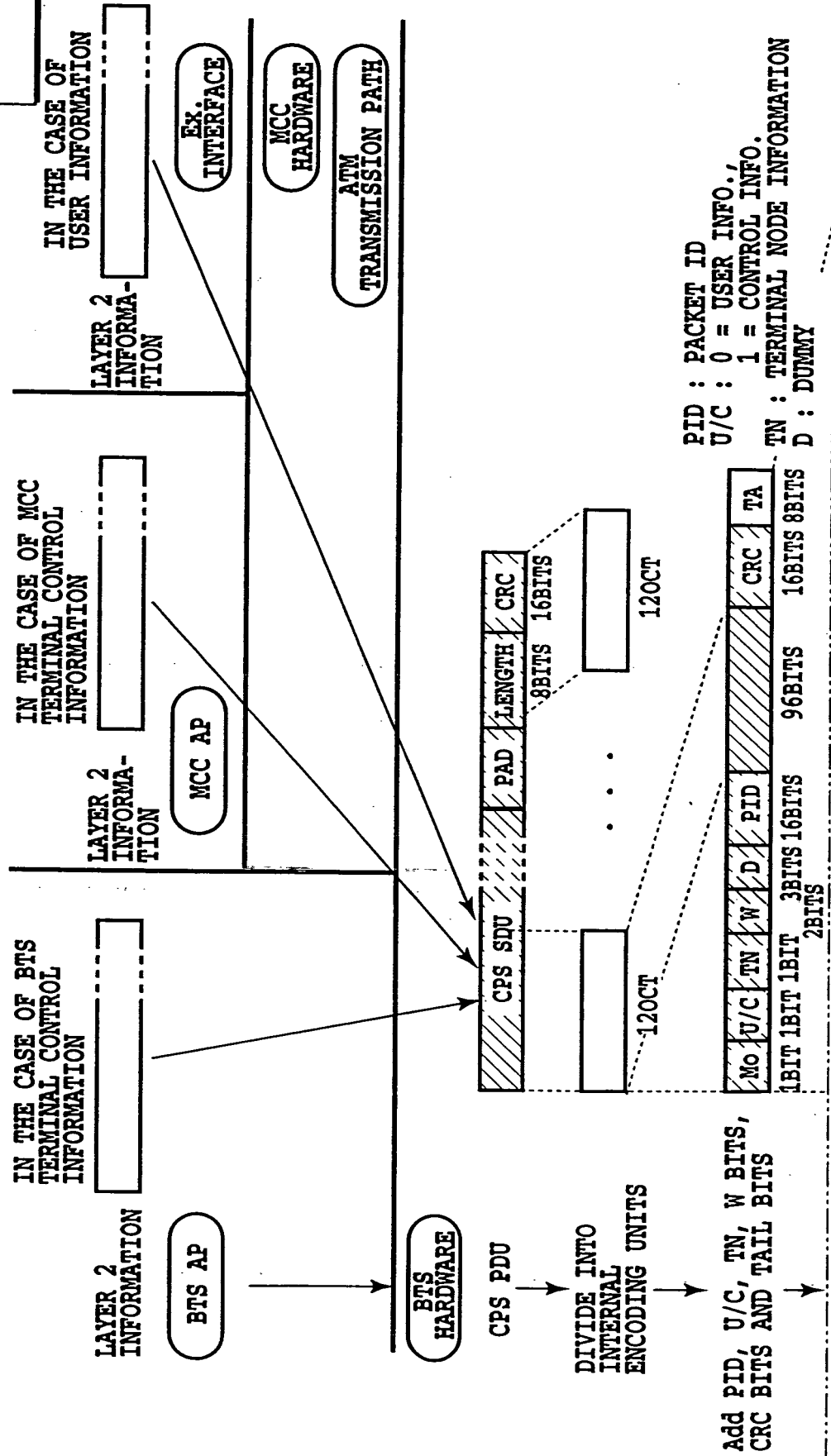
FIG.67

FIG.67A

FIG.67A

FIG.67B

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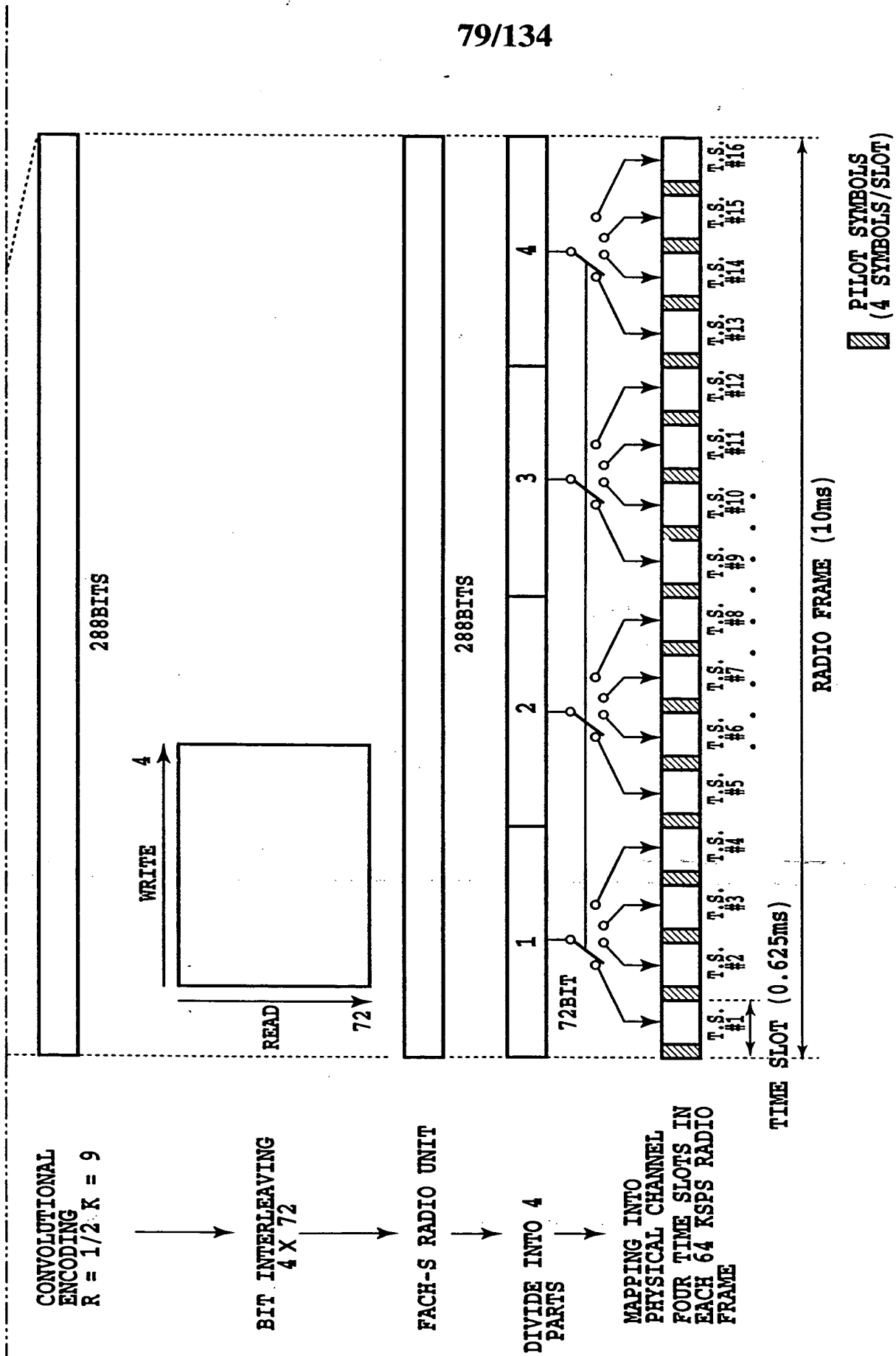


FIG.67B

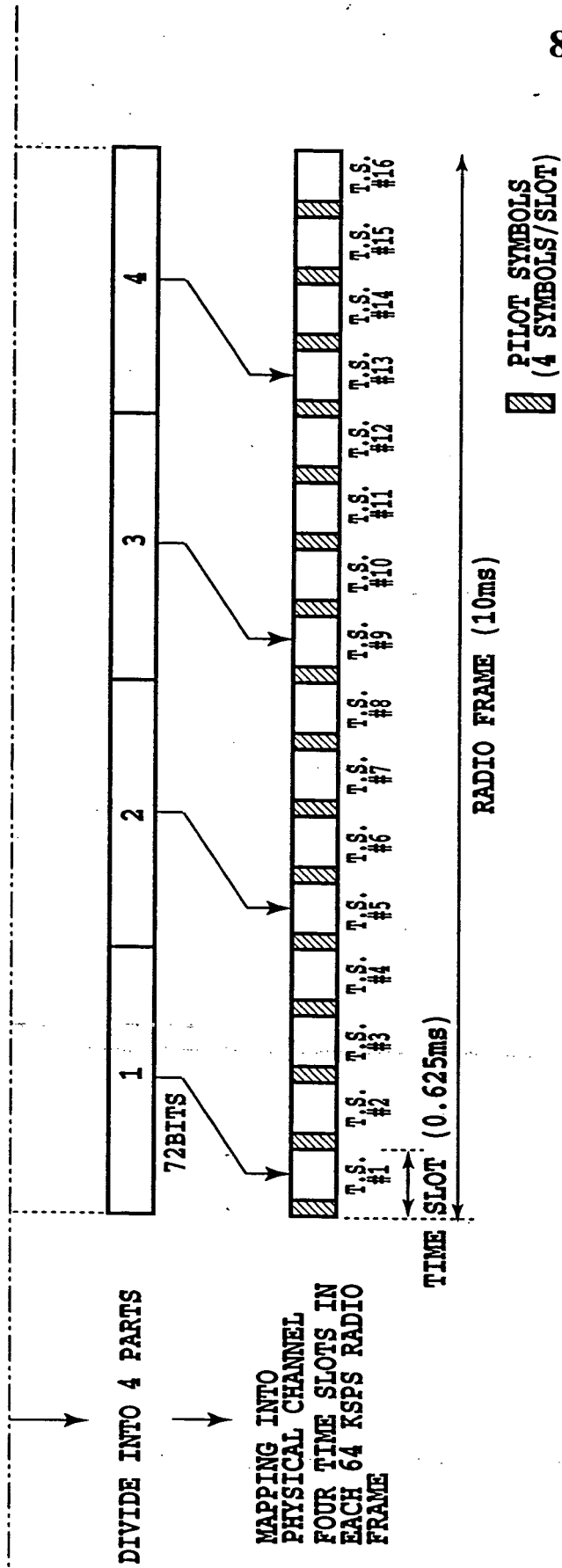


FIG.68B

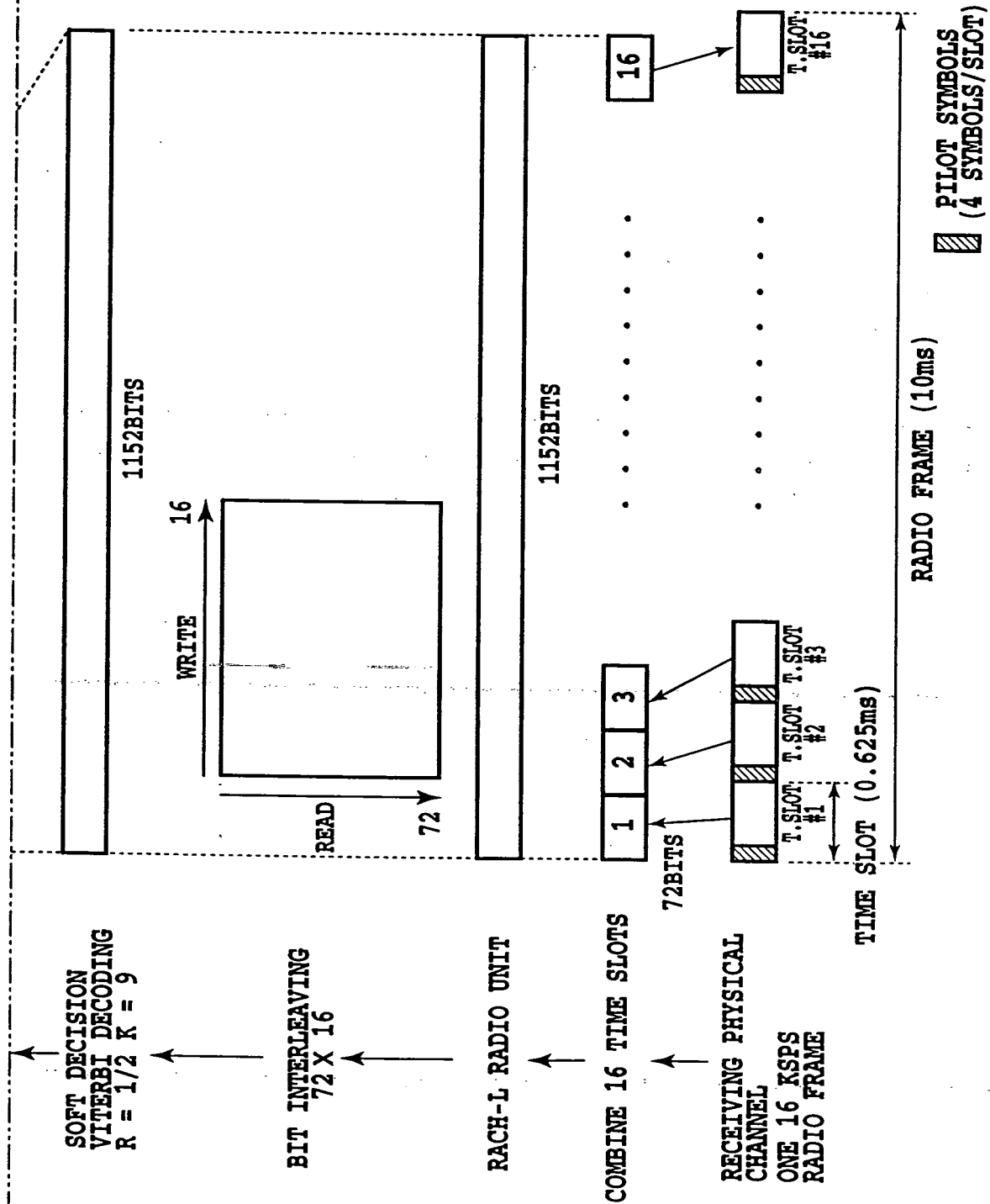


FIG.69B

FIG.70

FIG.70A

FIG.70B

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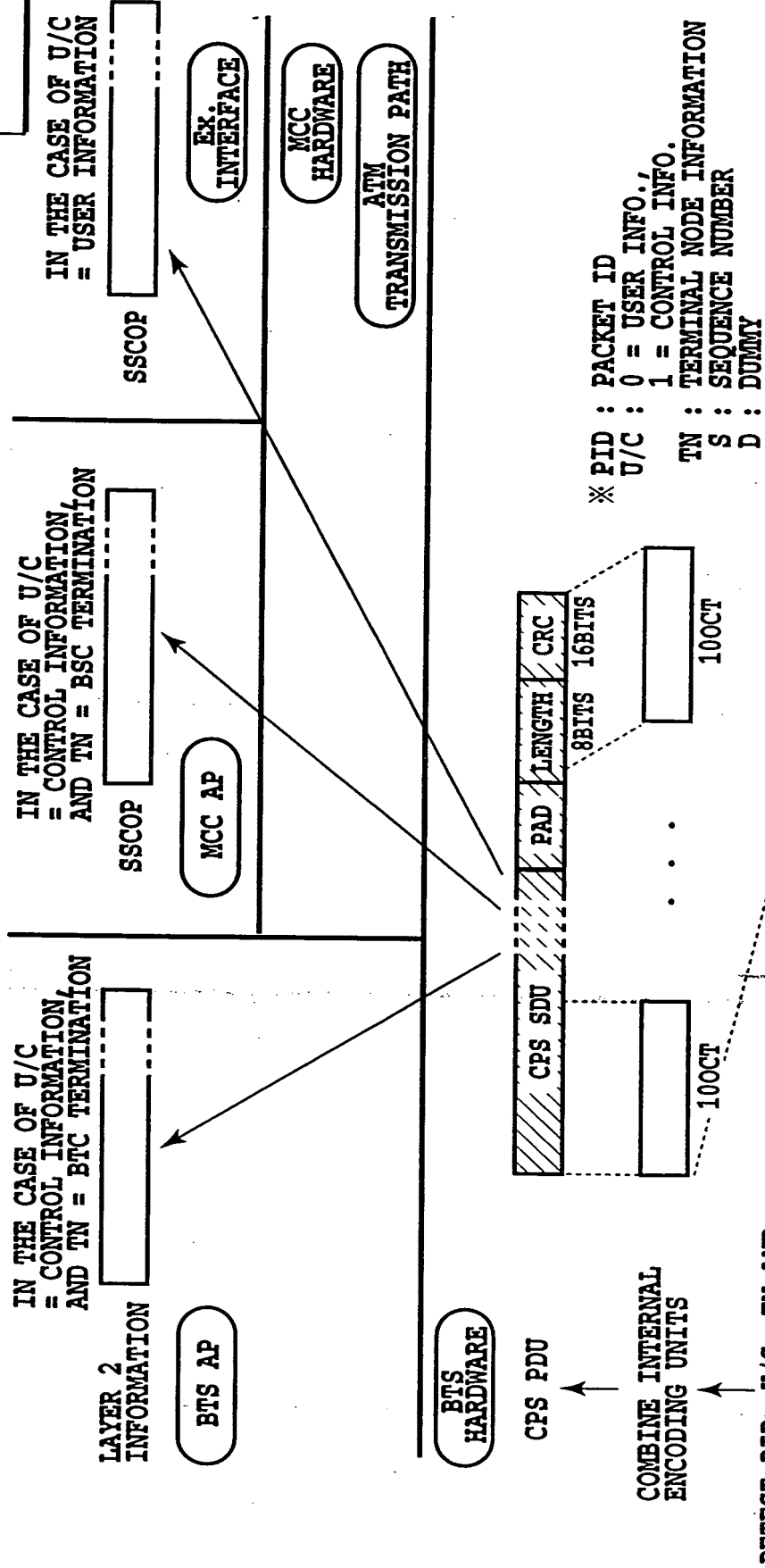


FIG.70A

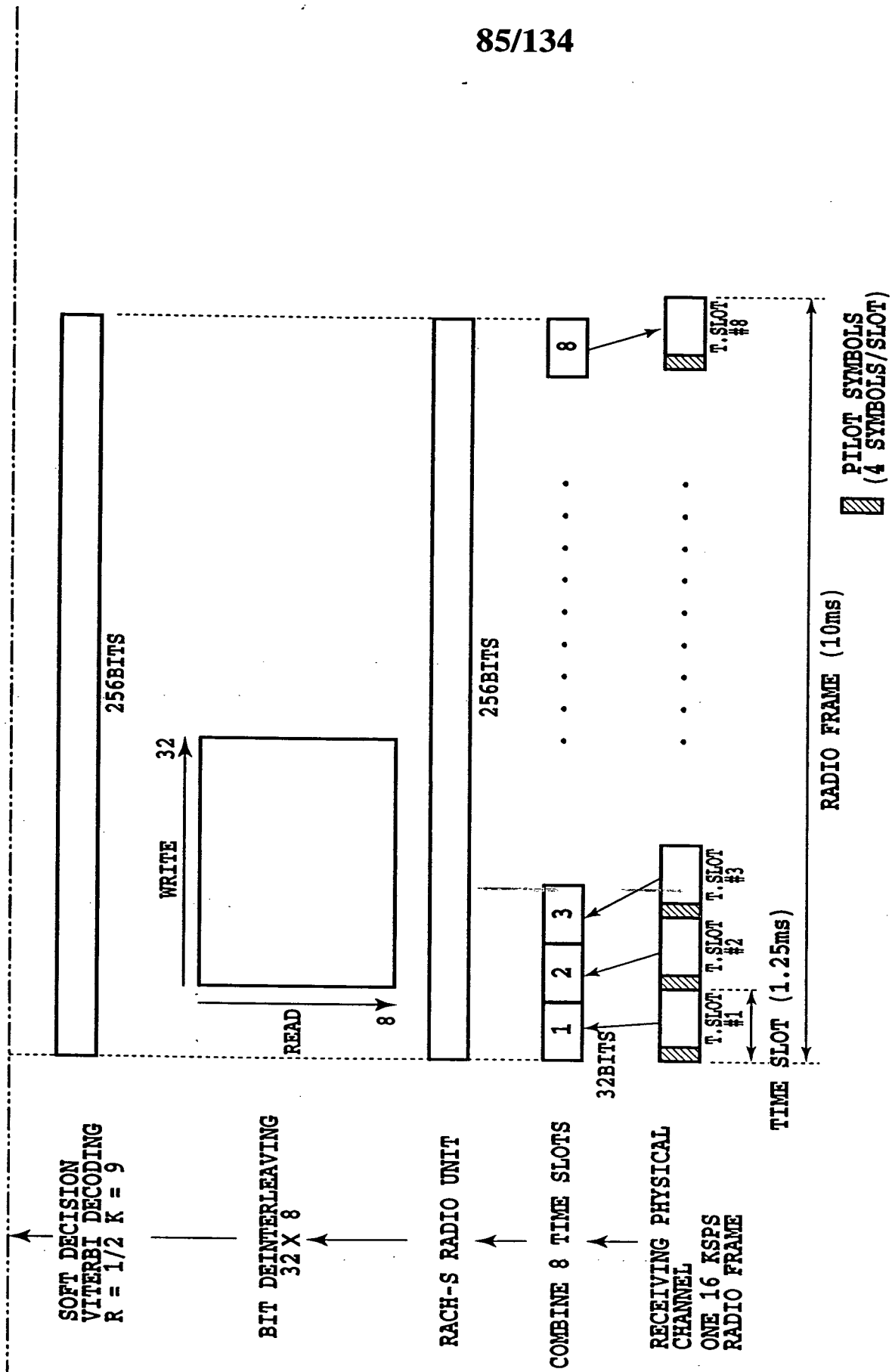


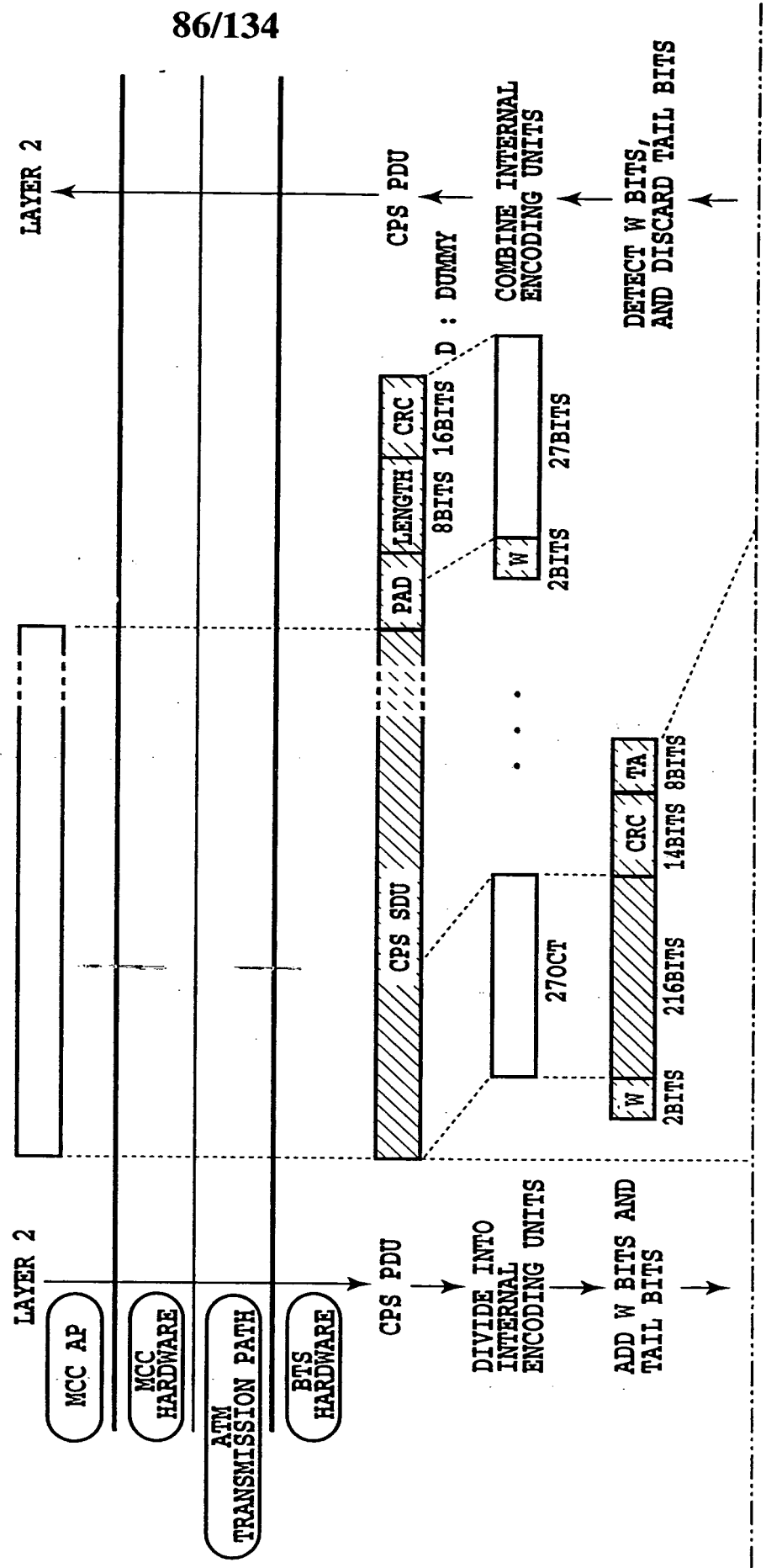
FIG.70B

FIG.71A

FIG.71

FIG.71A

FIG.71B



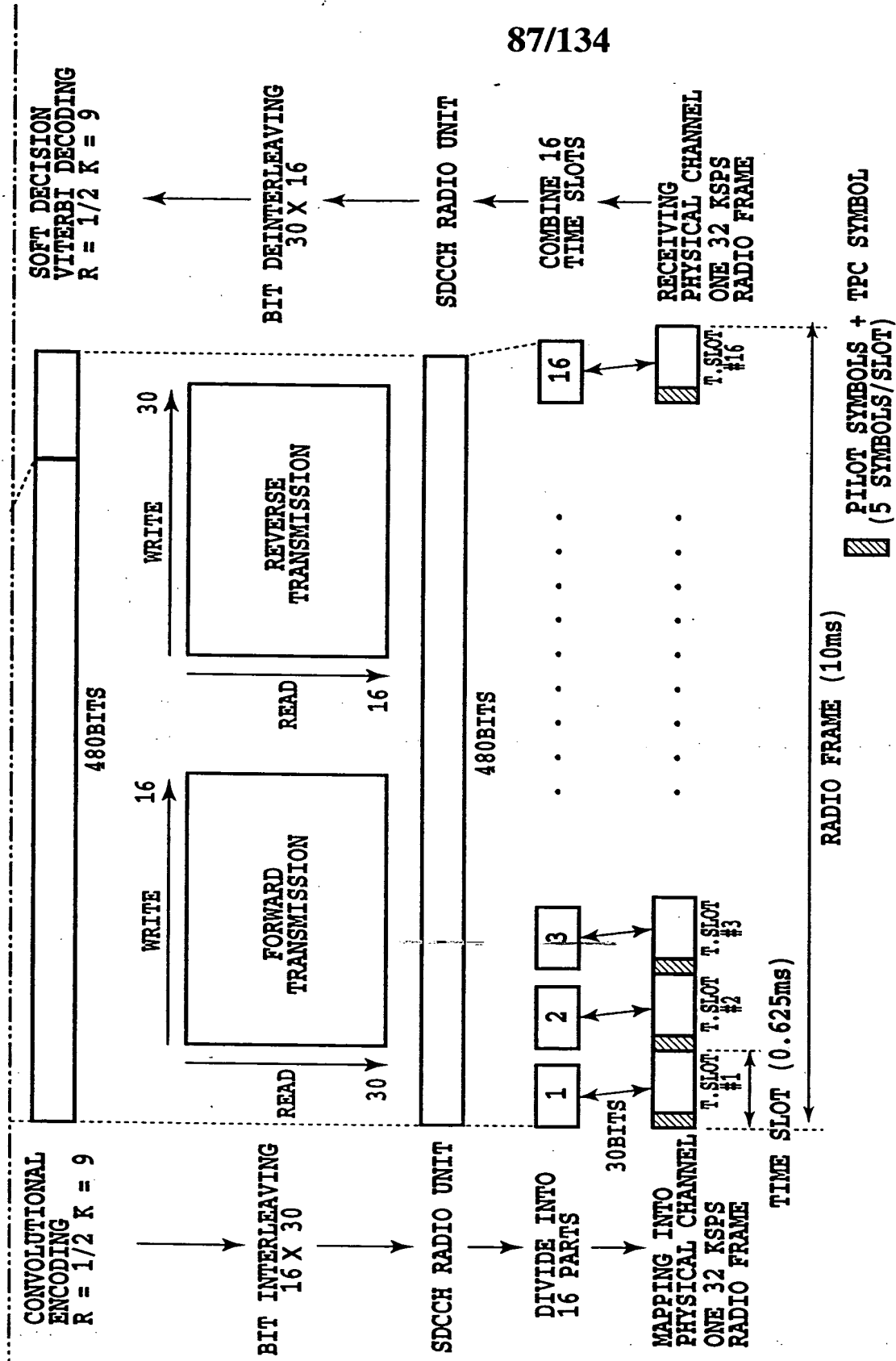


FIG. 71B

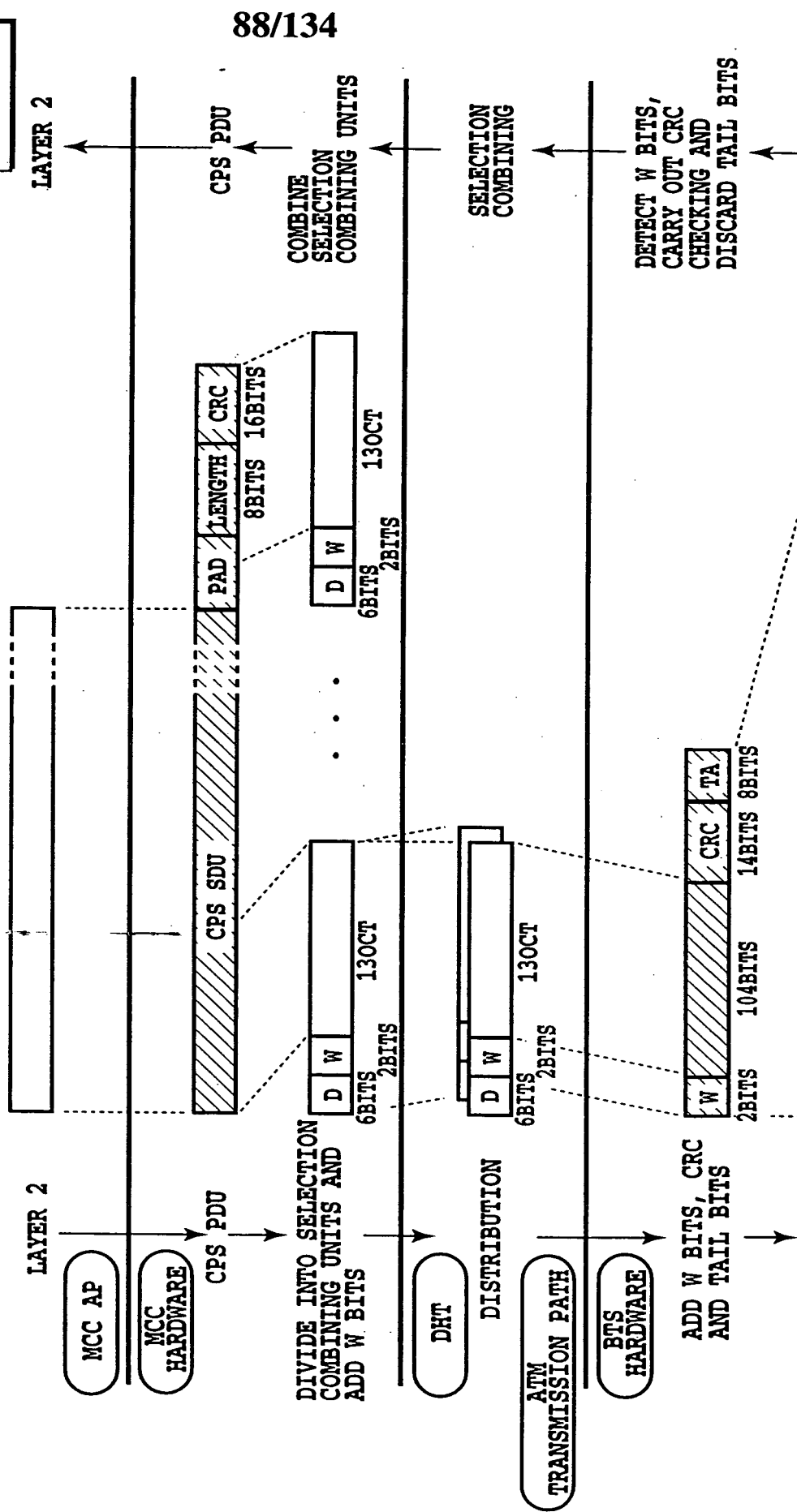
FIG.72

FIG.72A

FIG.72B

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FIG.72A



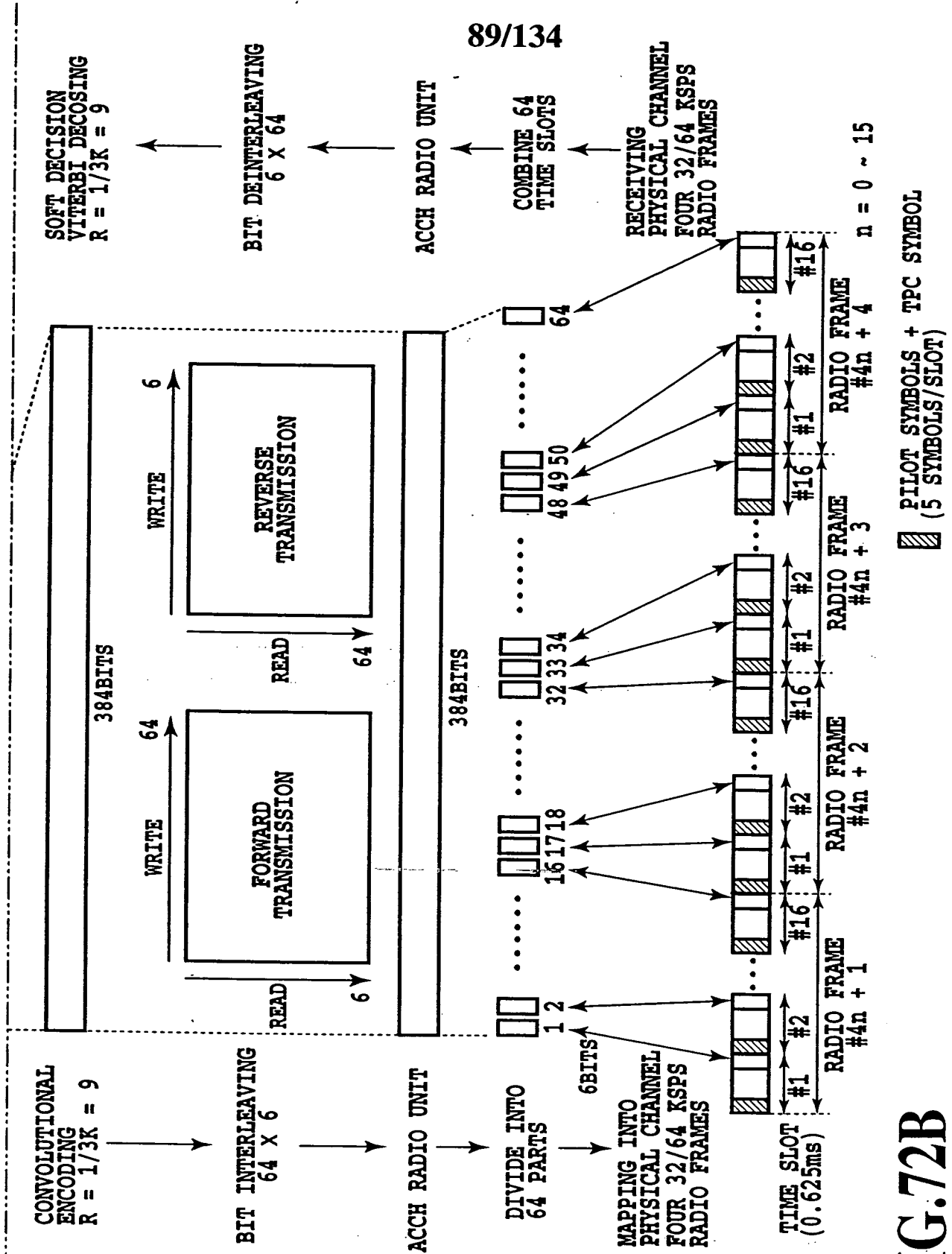


FIG.72B

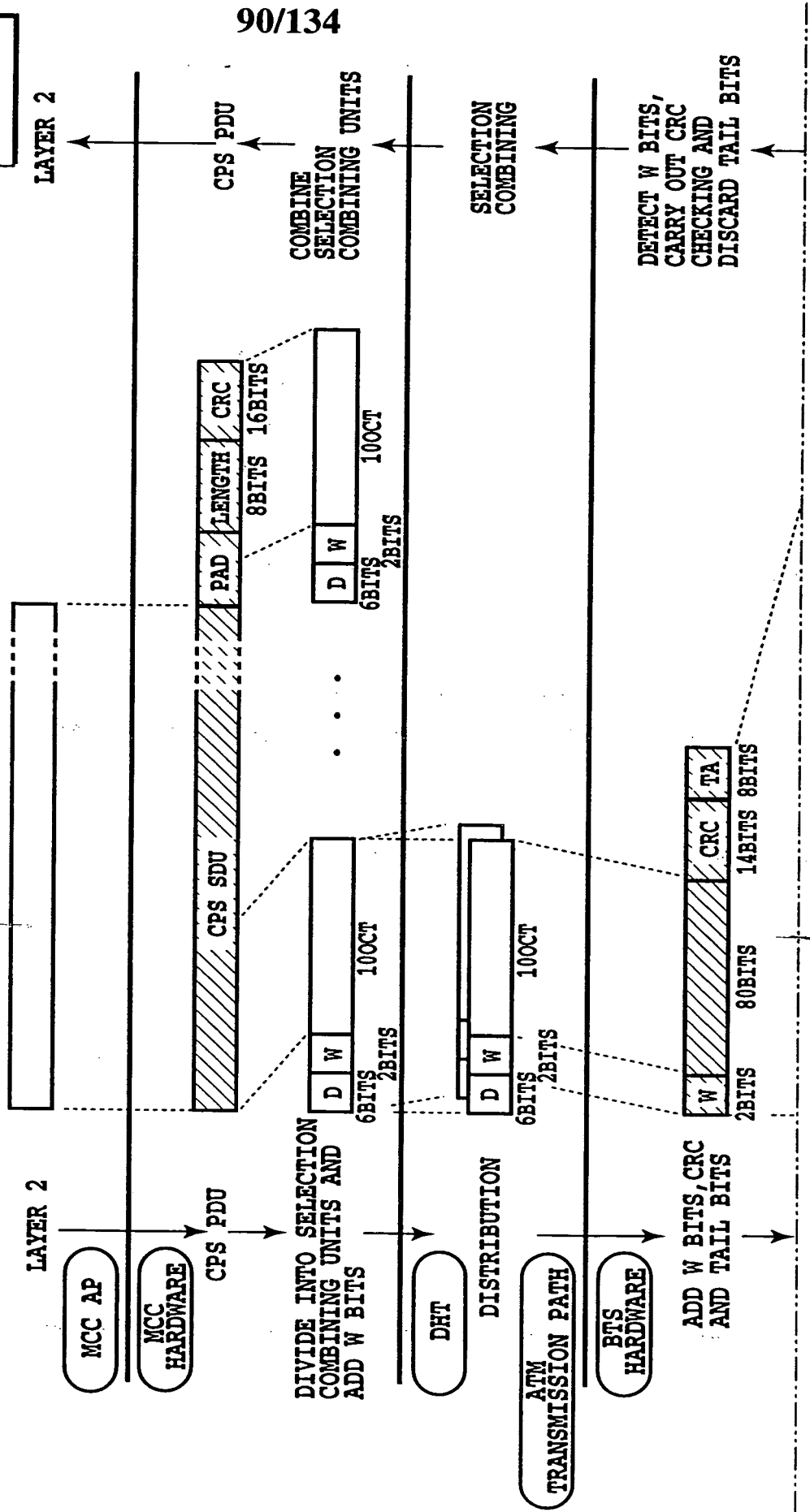
FIG.73

FIG.73A

FIG.73B

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FIG.73A



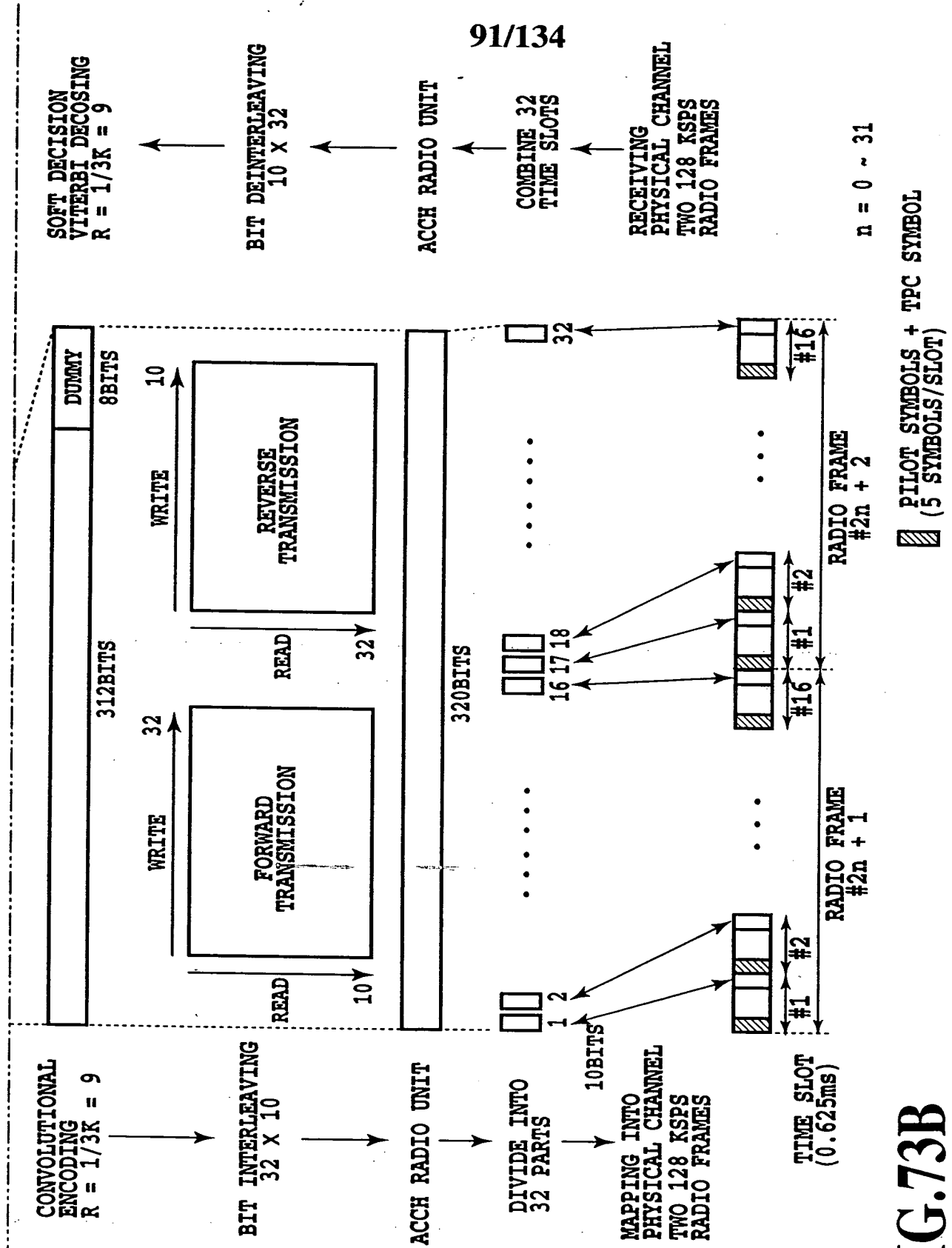


FIG.73B

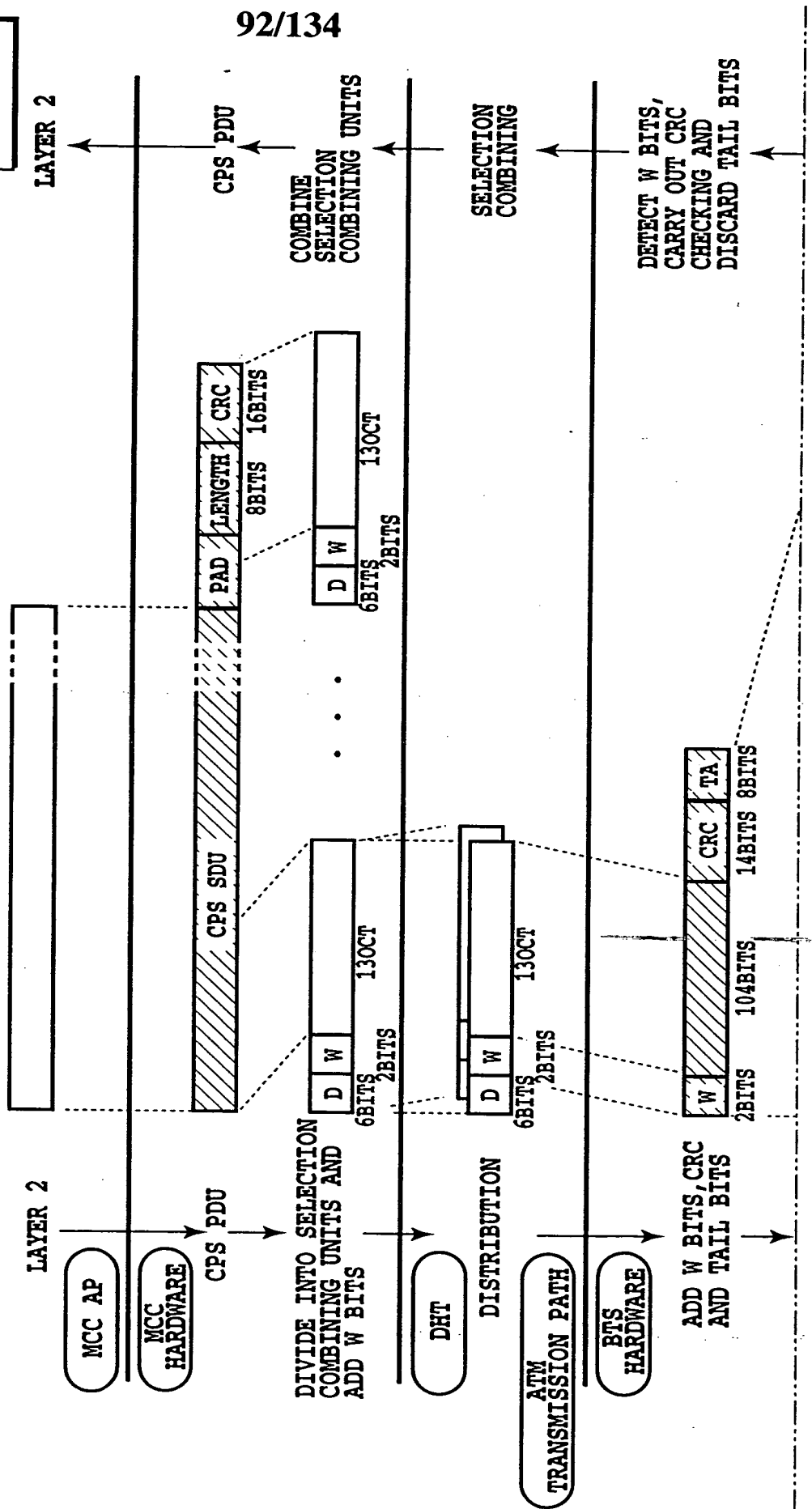
FIG.74

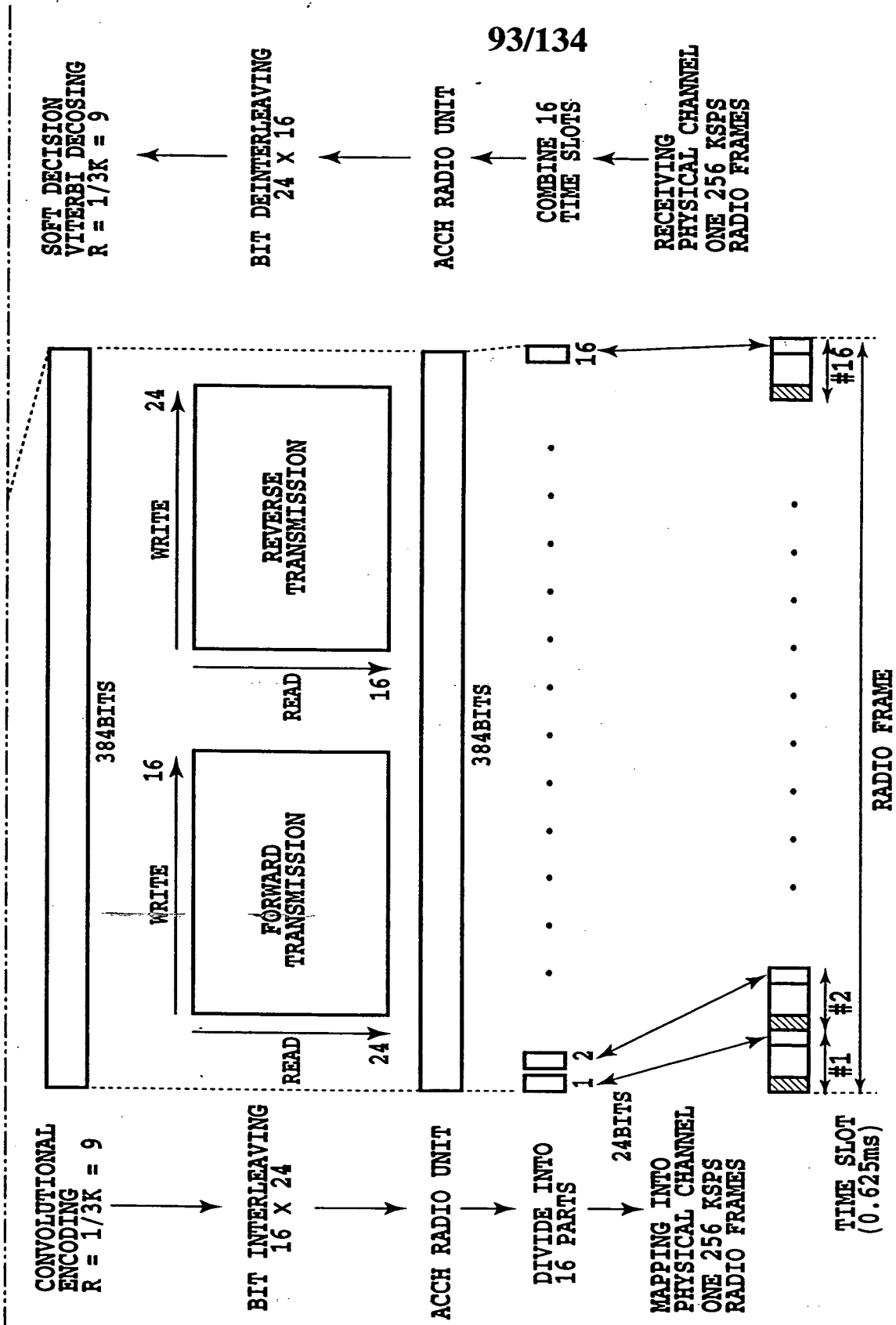
FIG.74A

FIG.74B

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FIG.74A





 **PILOT SYMBOLS + TPC SYMBOL**
 (9 SYMBOLS/SLOT)

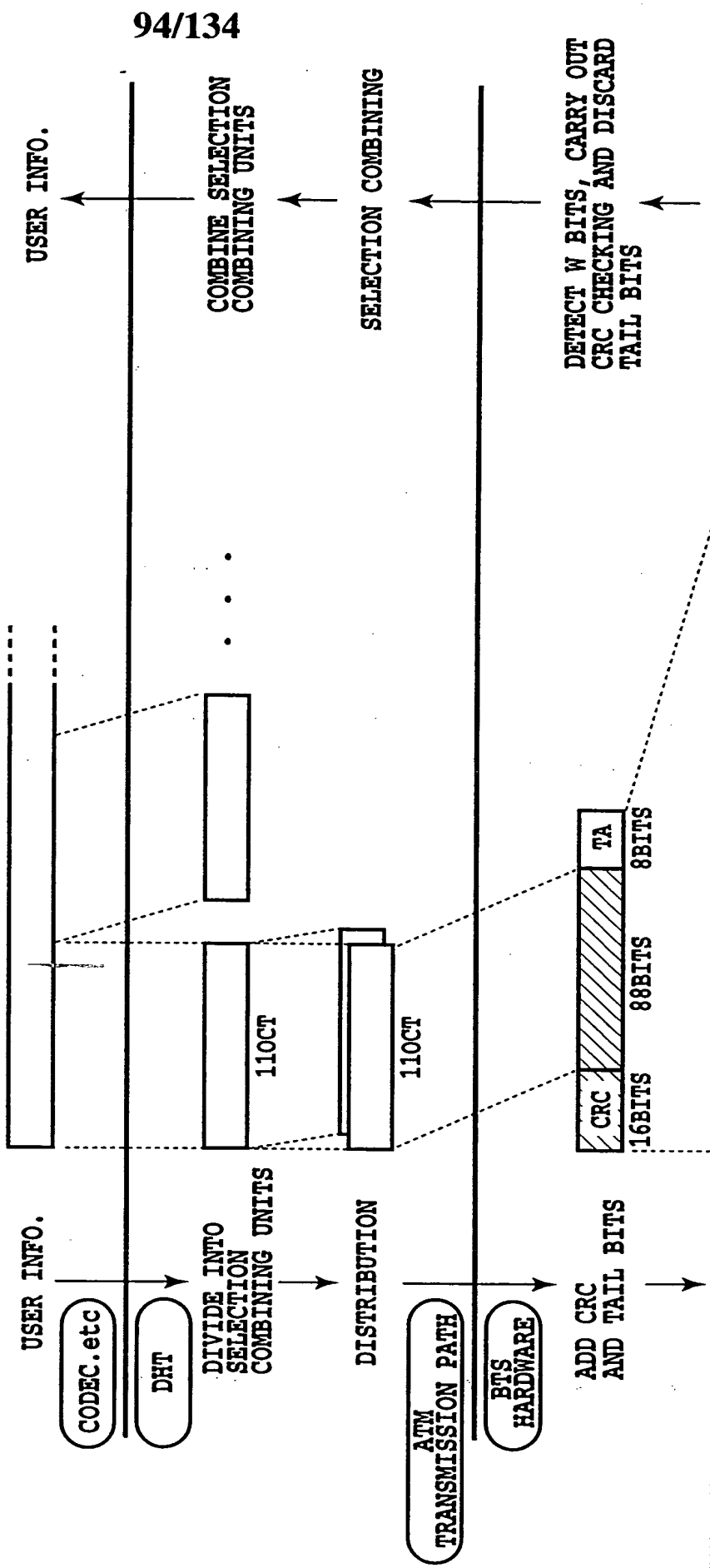
FIG.74B

FIG.75

FIG.75A

FIG.75B

FIG.75A



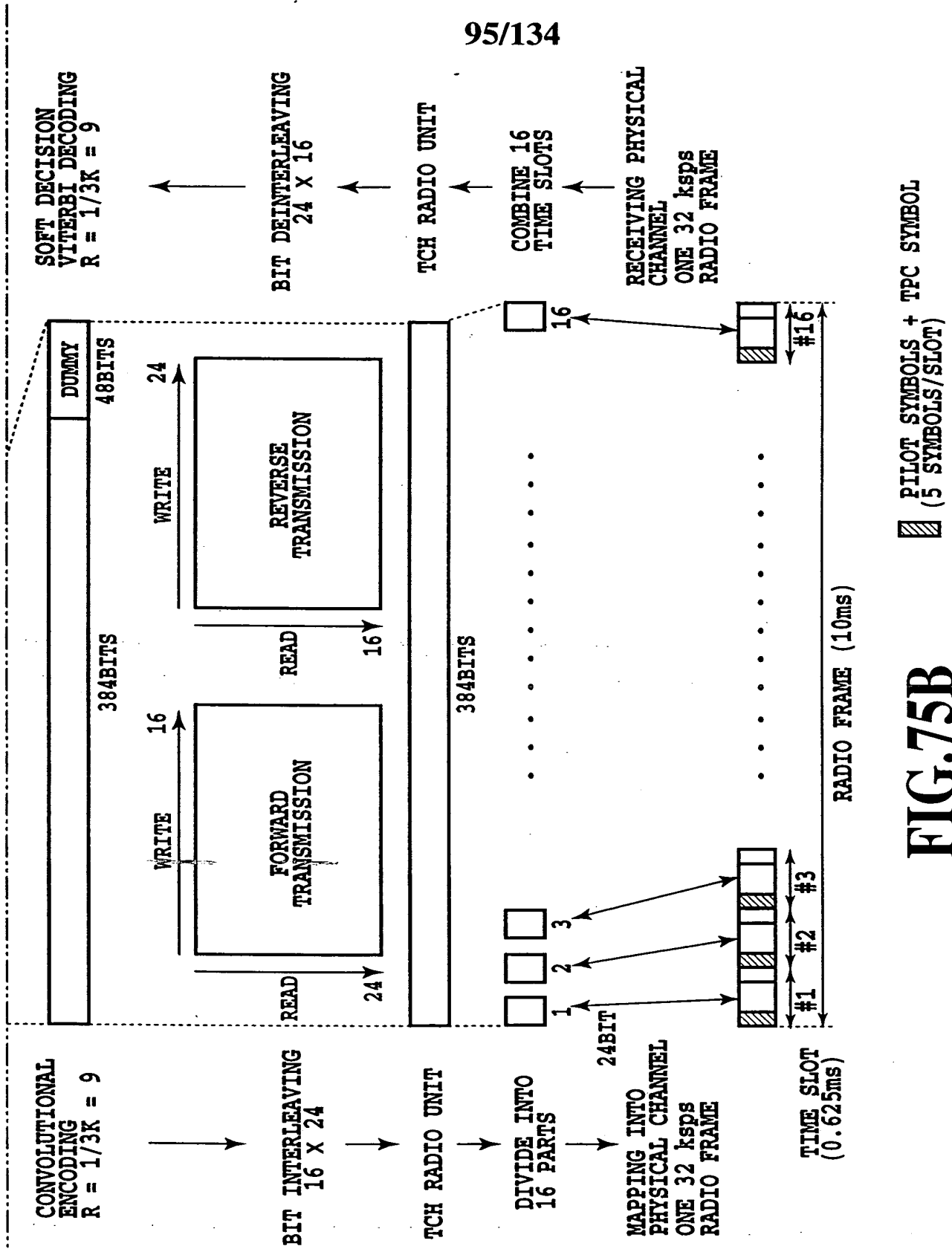


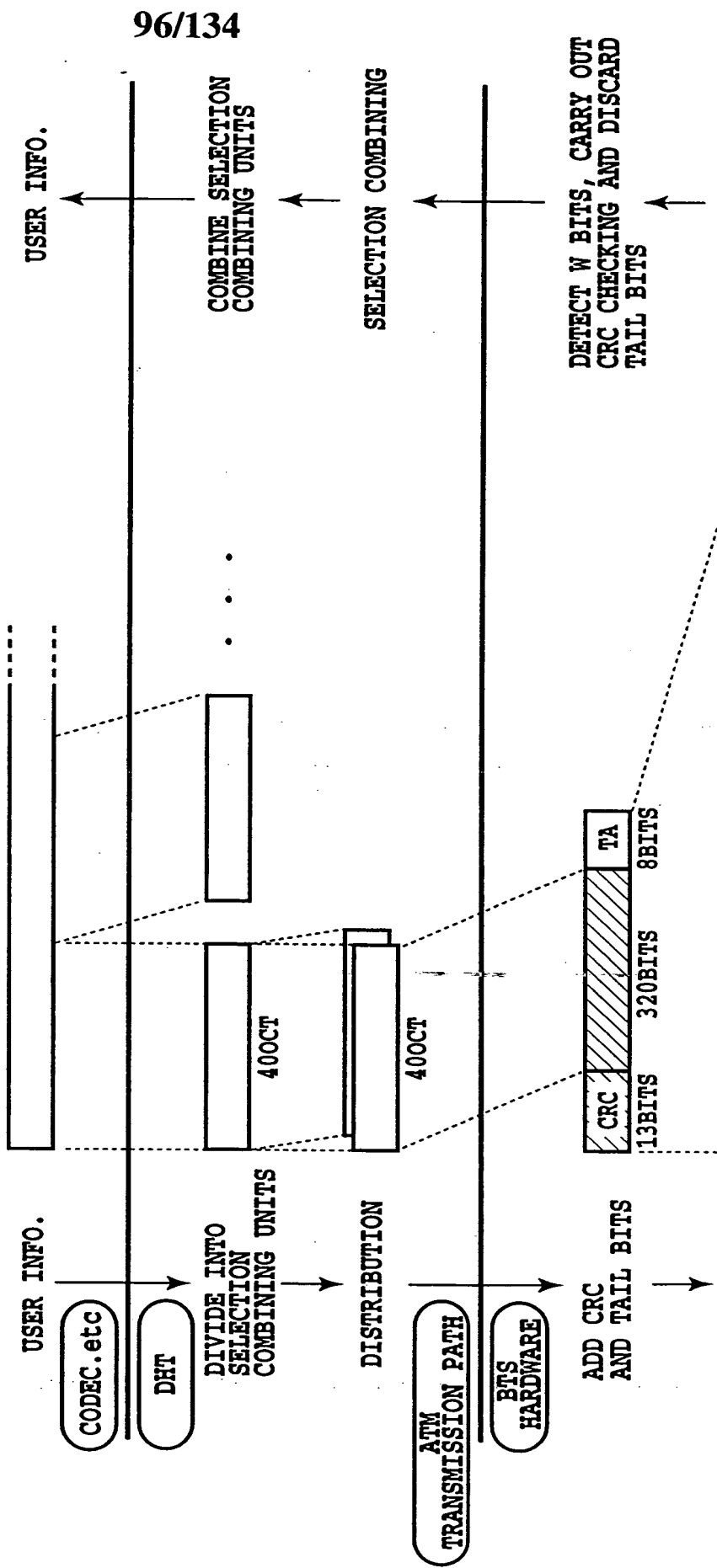
FIG.75B

FIG.76

FIG.76A

FIG.76B

FIG.76A



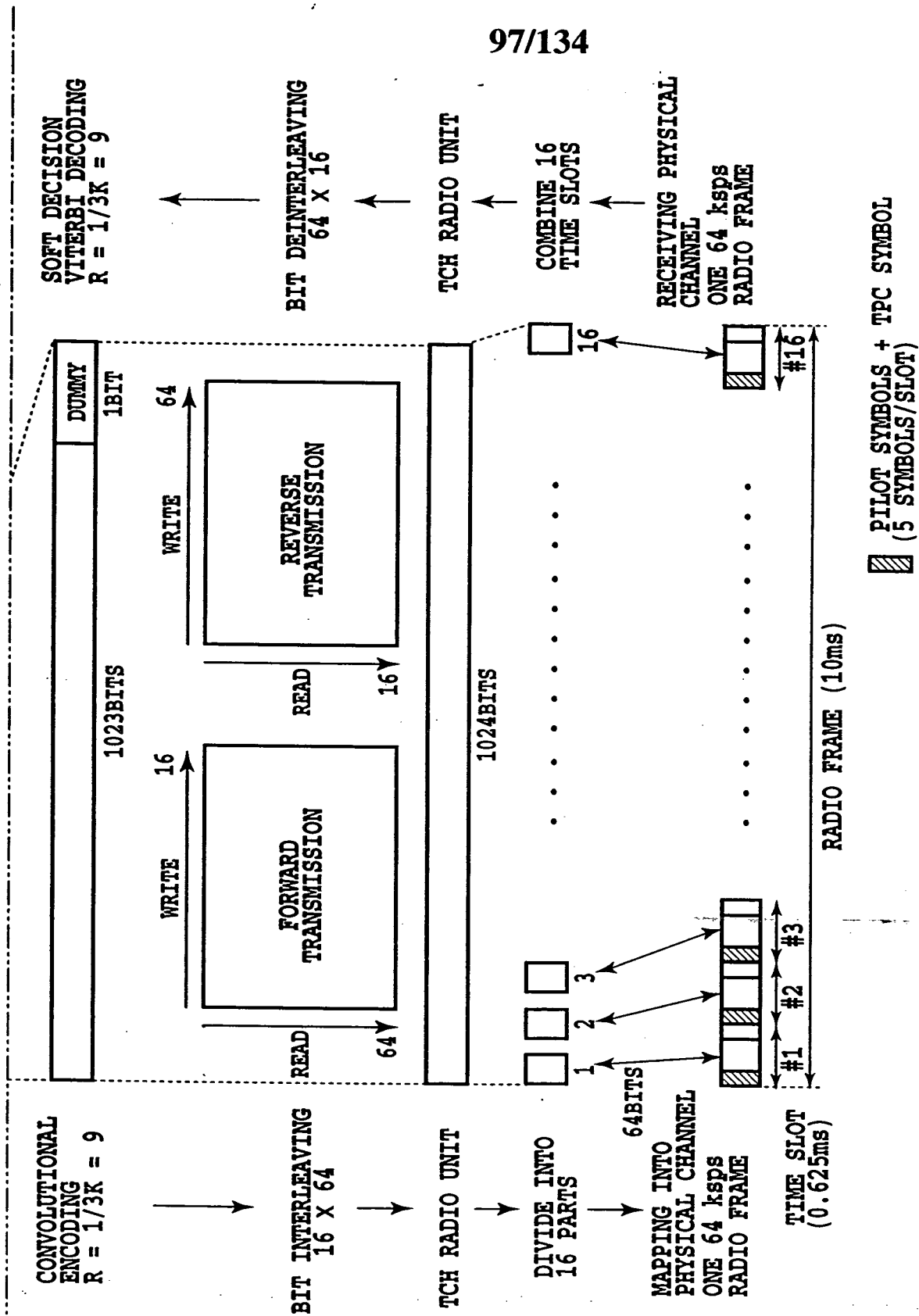


FIG.76B

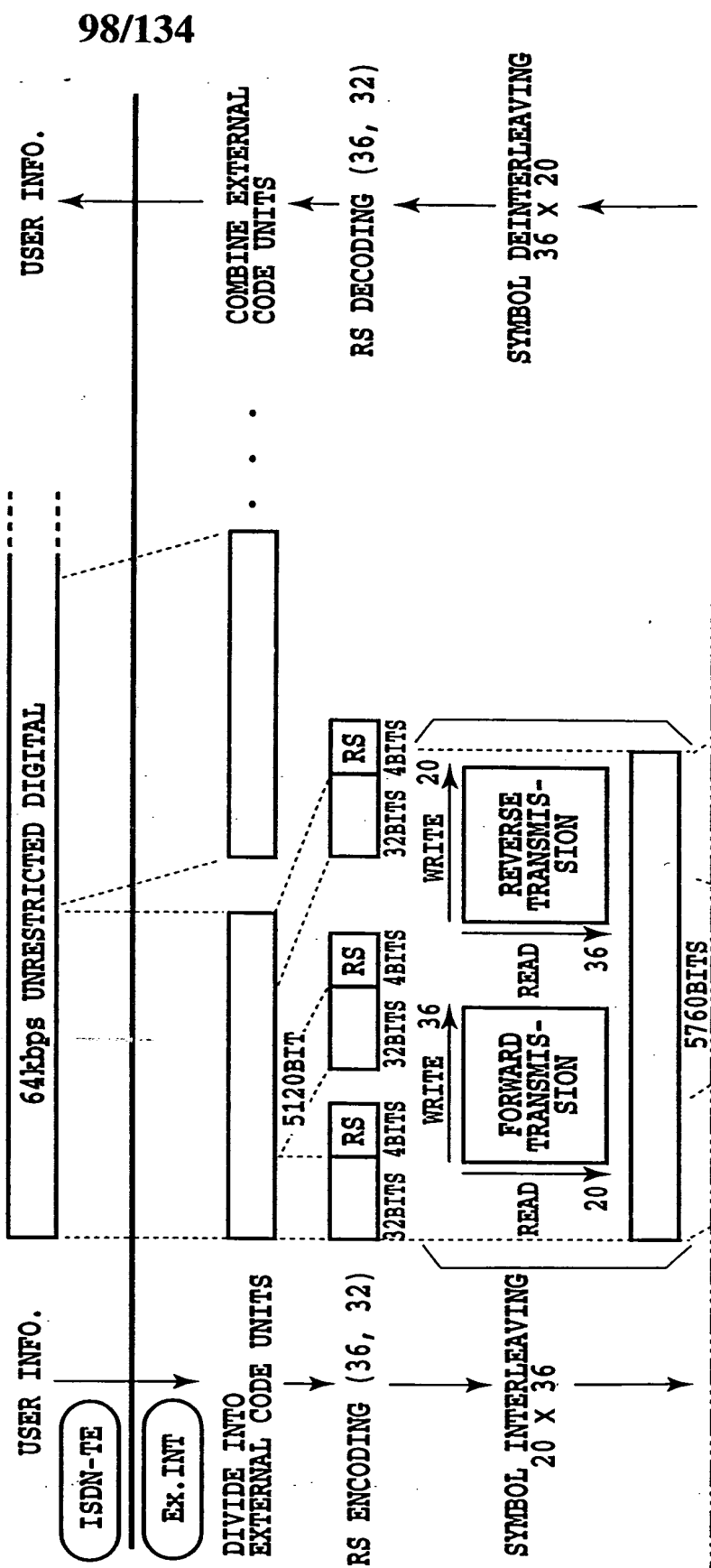
FIG.77

FIG.77A

FIG.77B

FIG.77C

FIG.77A



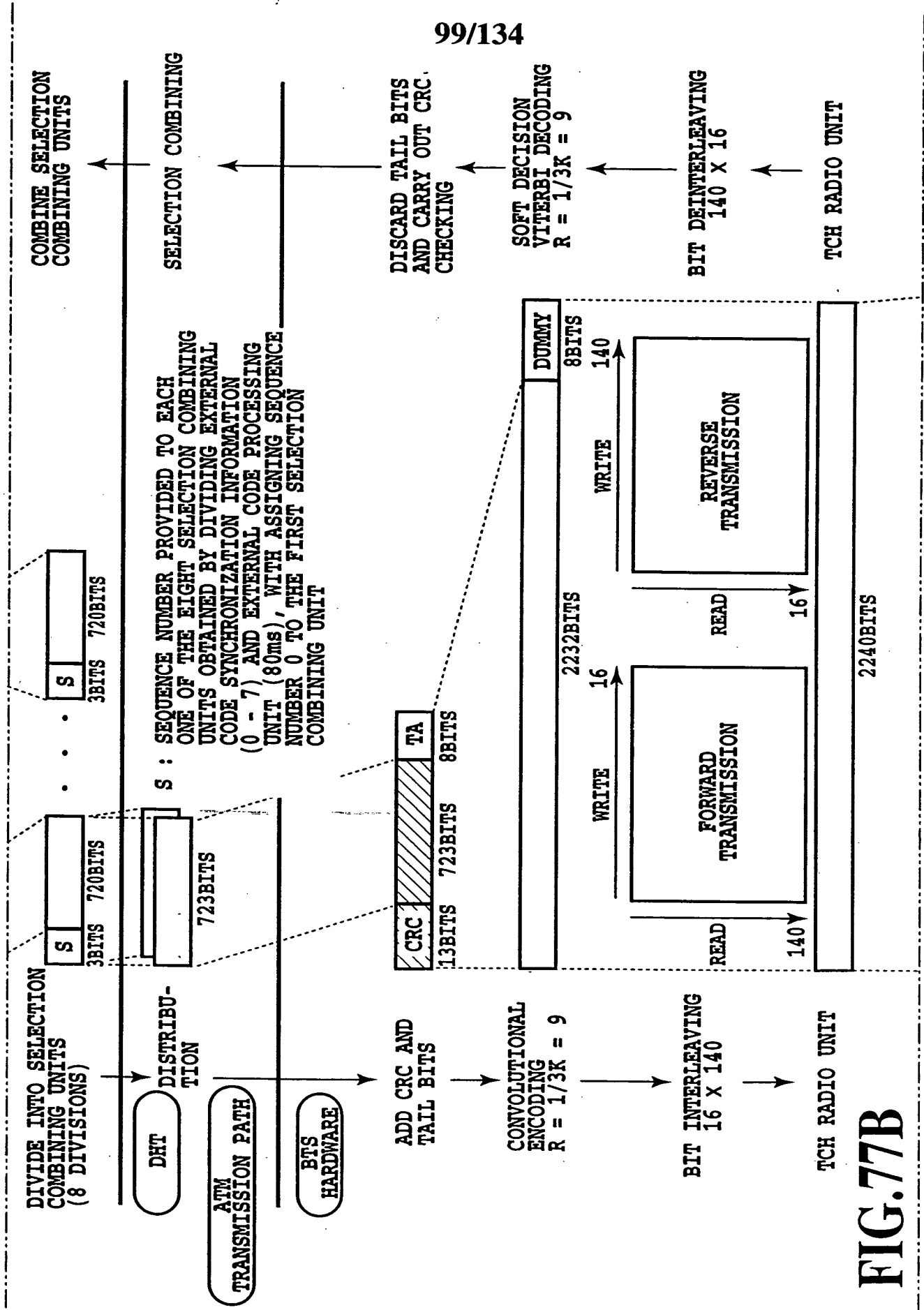


FIG.77B

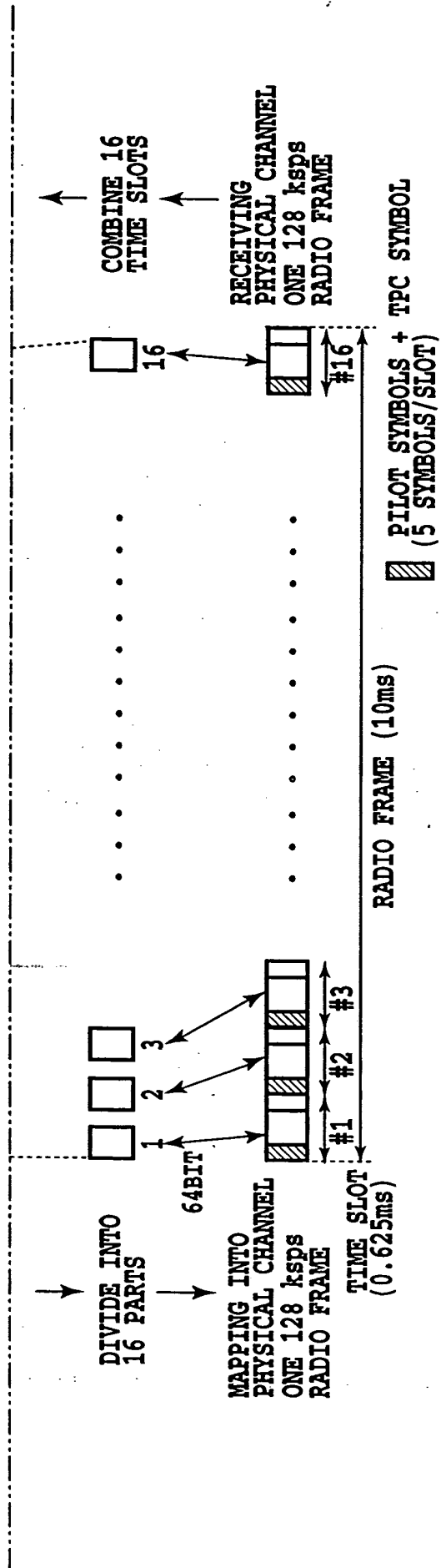


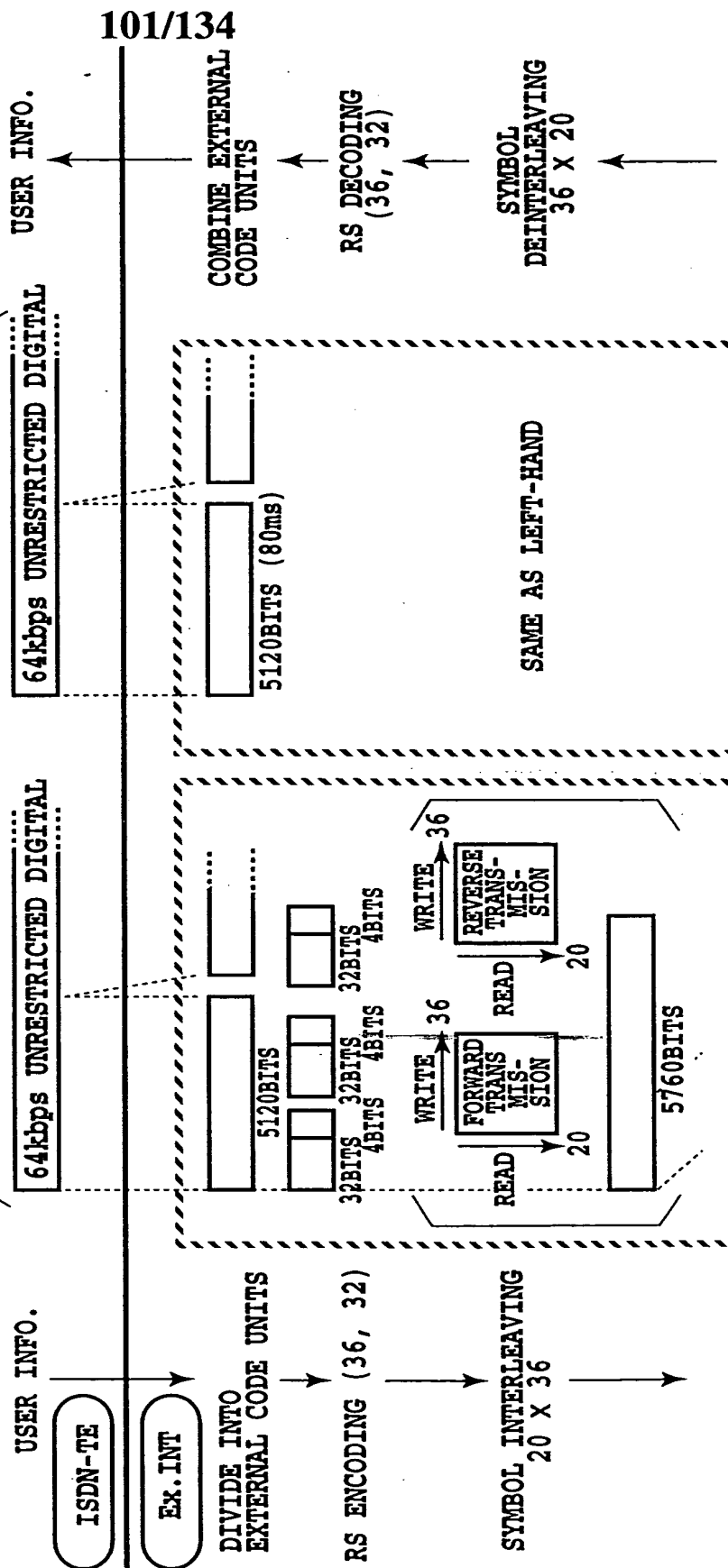
FIG.77C

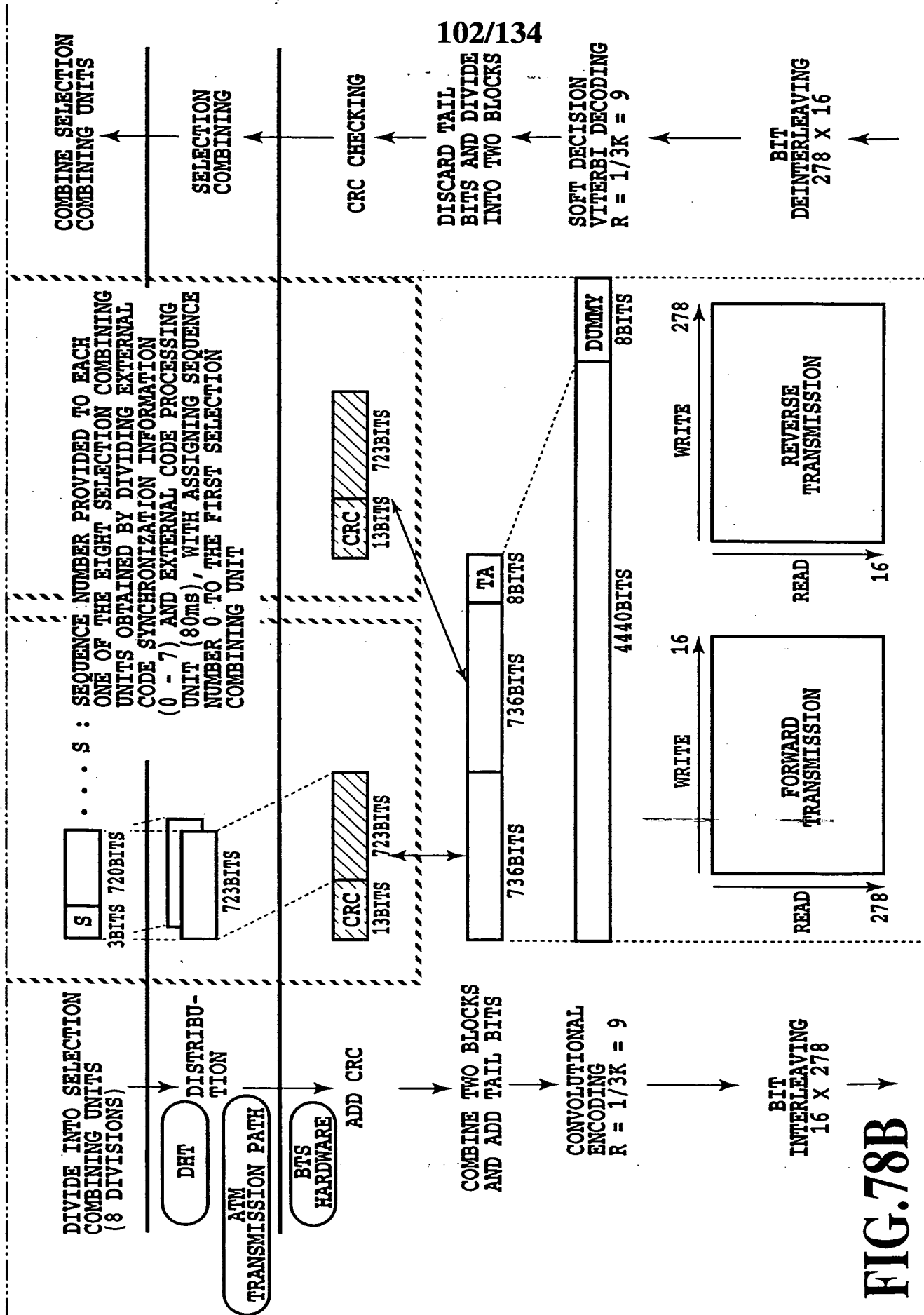
FIG.78

FIG.78A
FIG.78B
FIG.78C

FIG.78A

2B = 128kbps





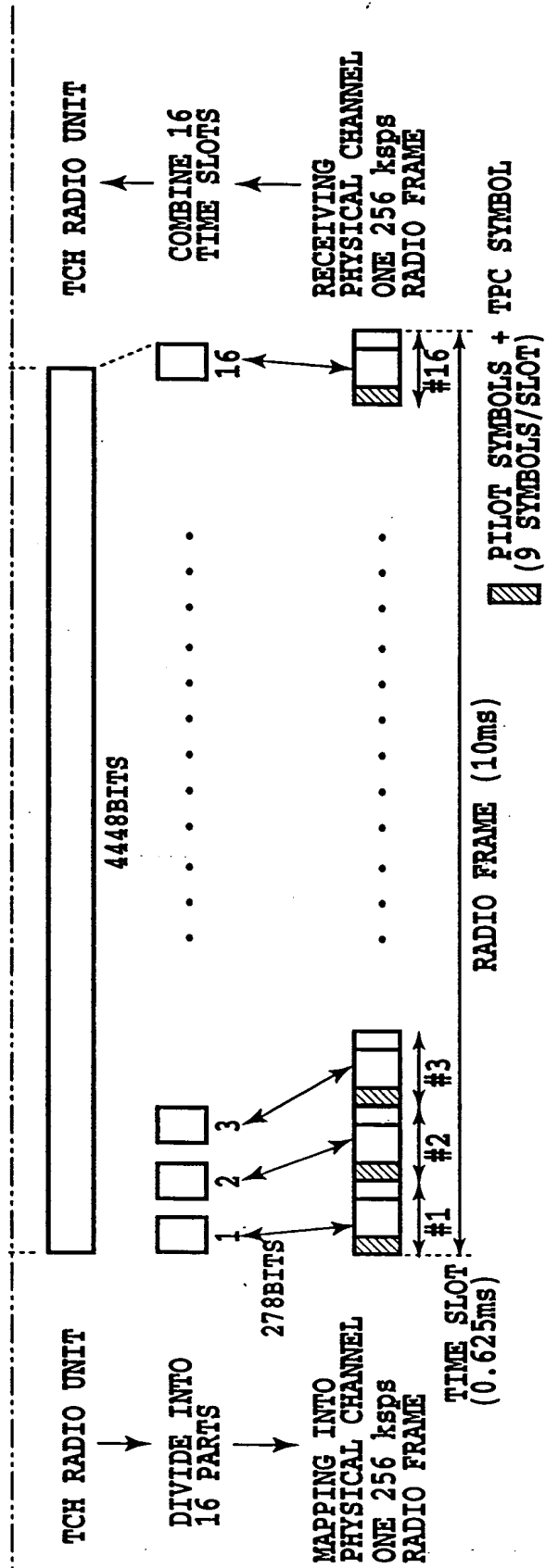


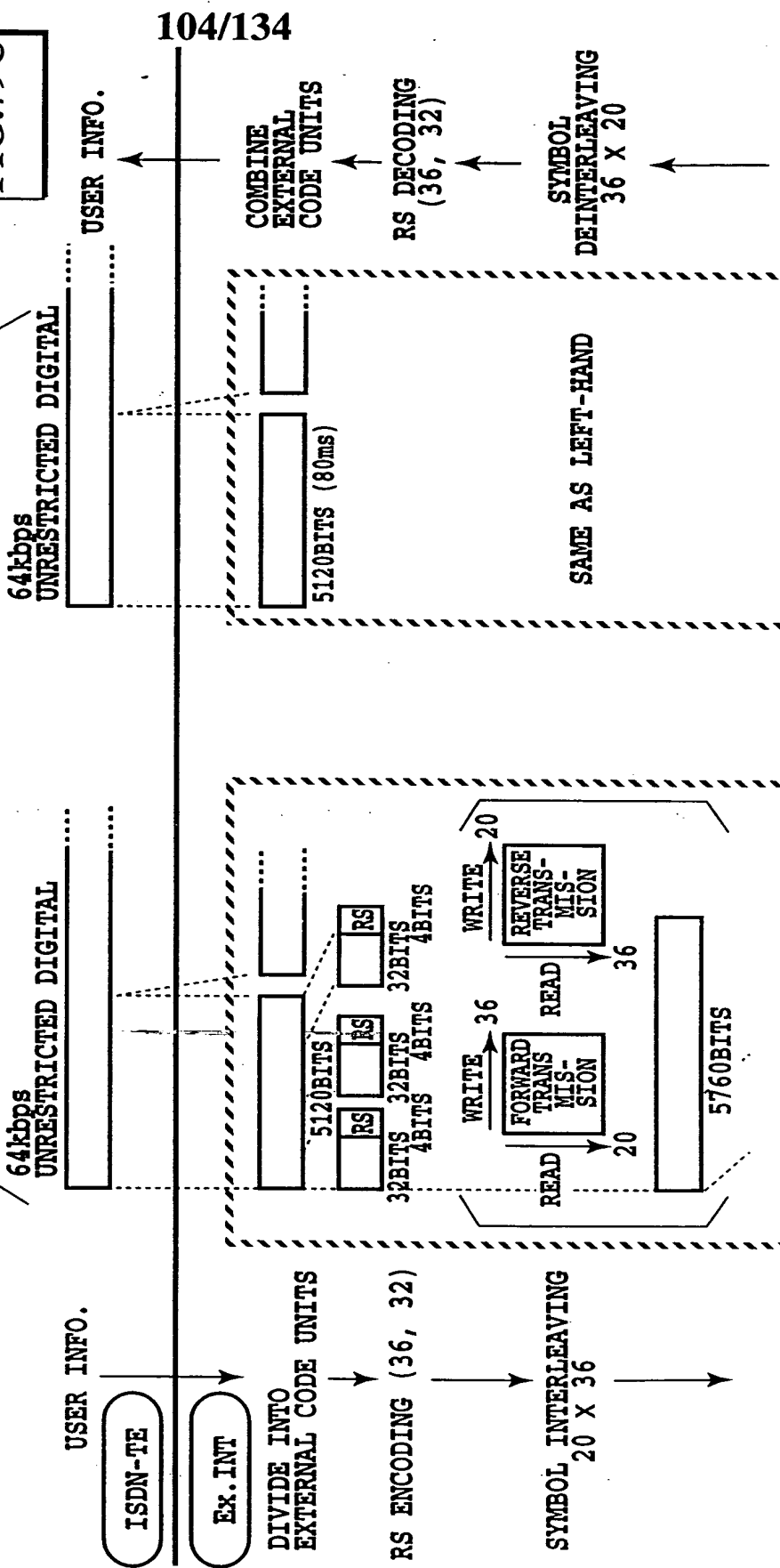
FIG.78C

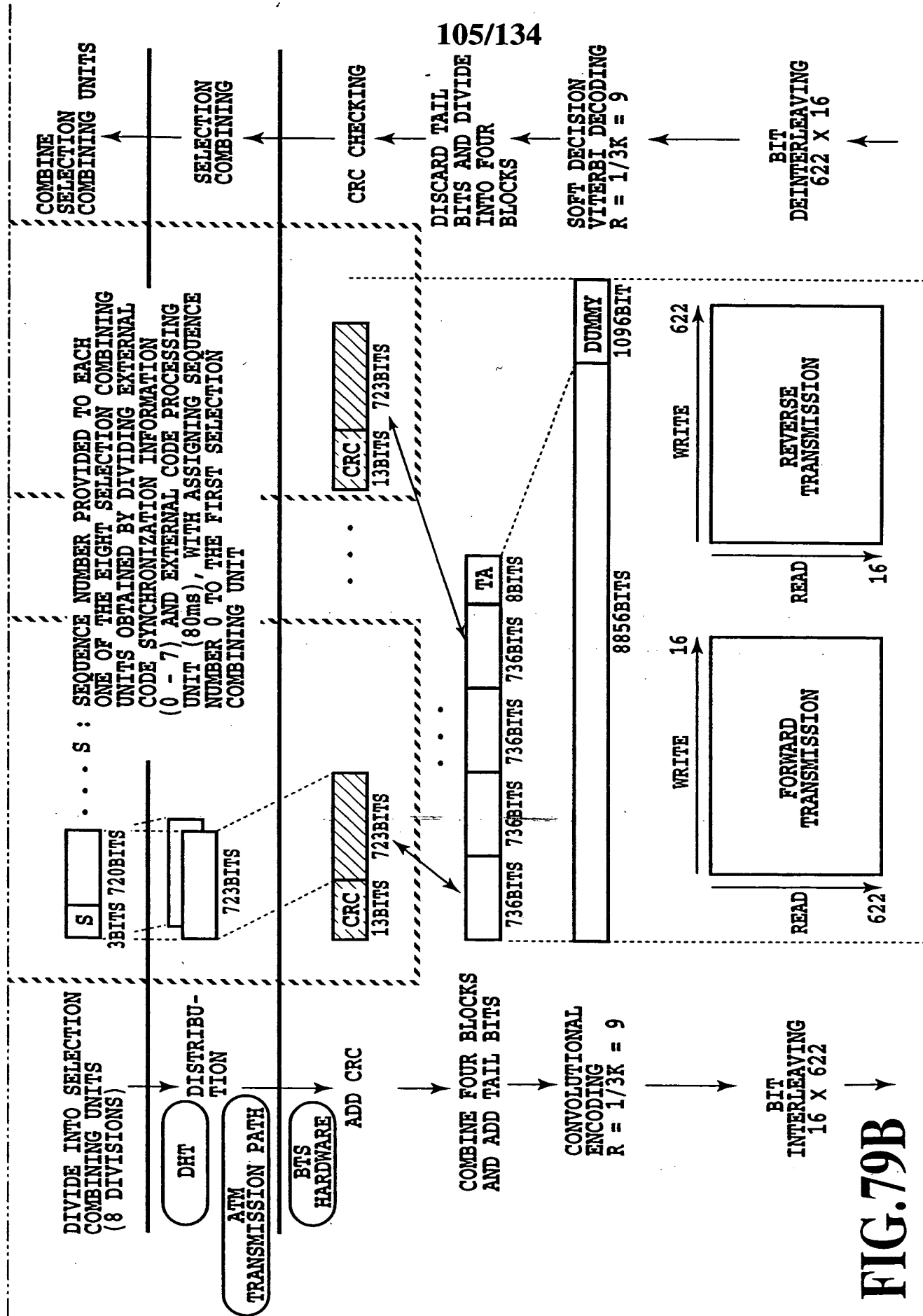
FIG.79

FIG.79A
FIG.79B
FIG.79C

FIG.79A

4B = 256kbps





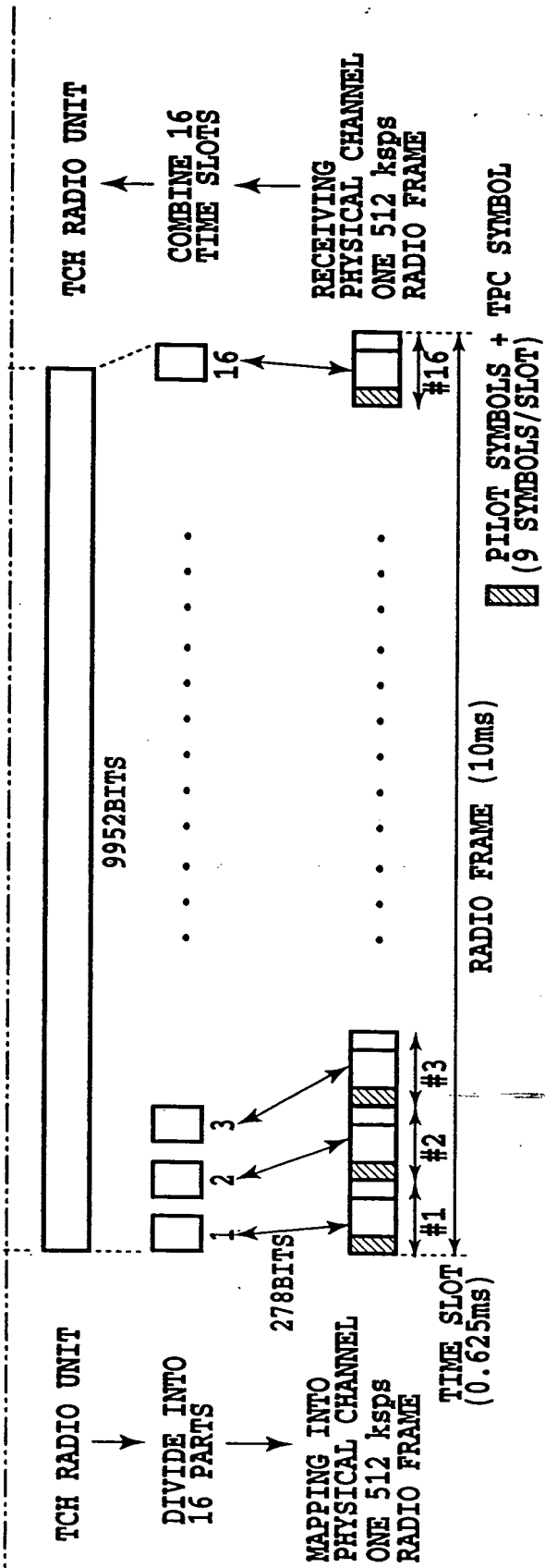


FIG.79C

FIG.80

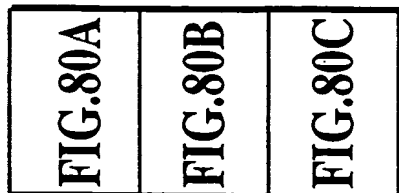
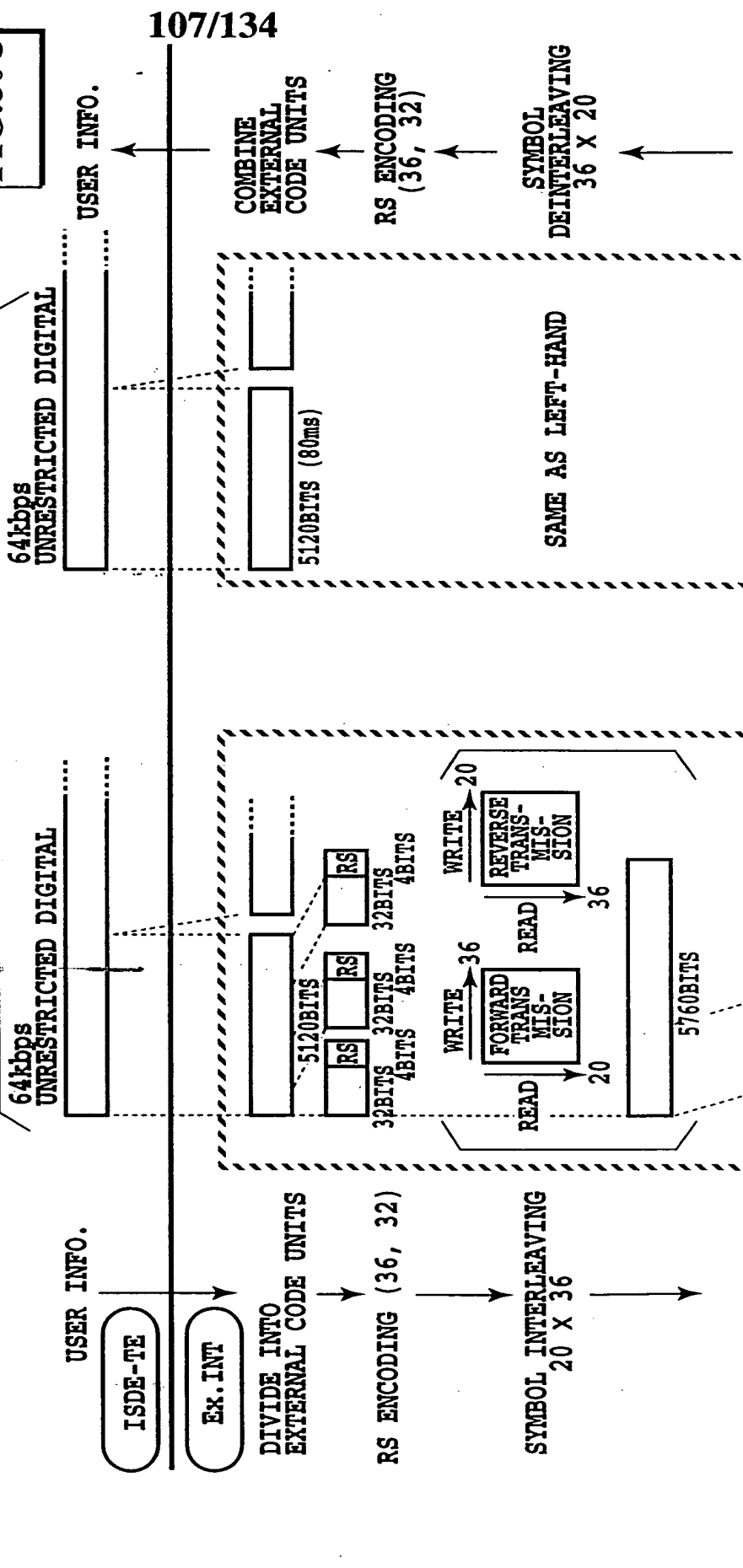
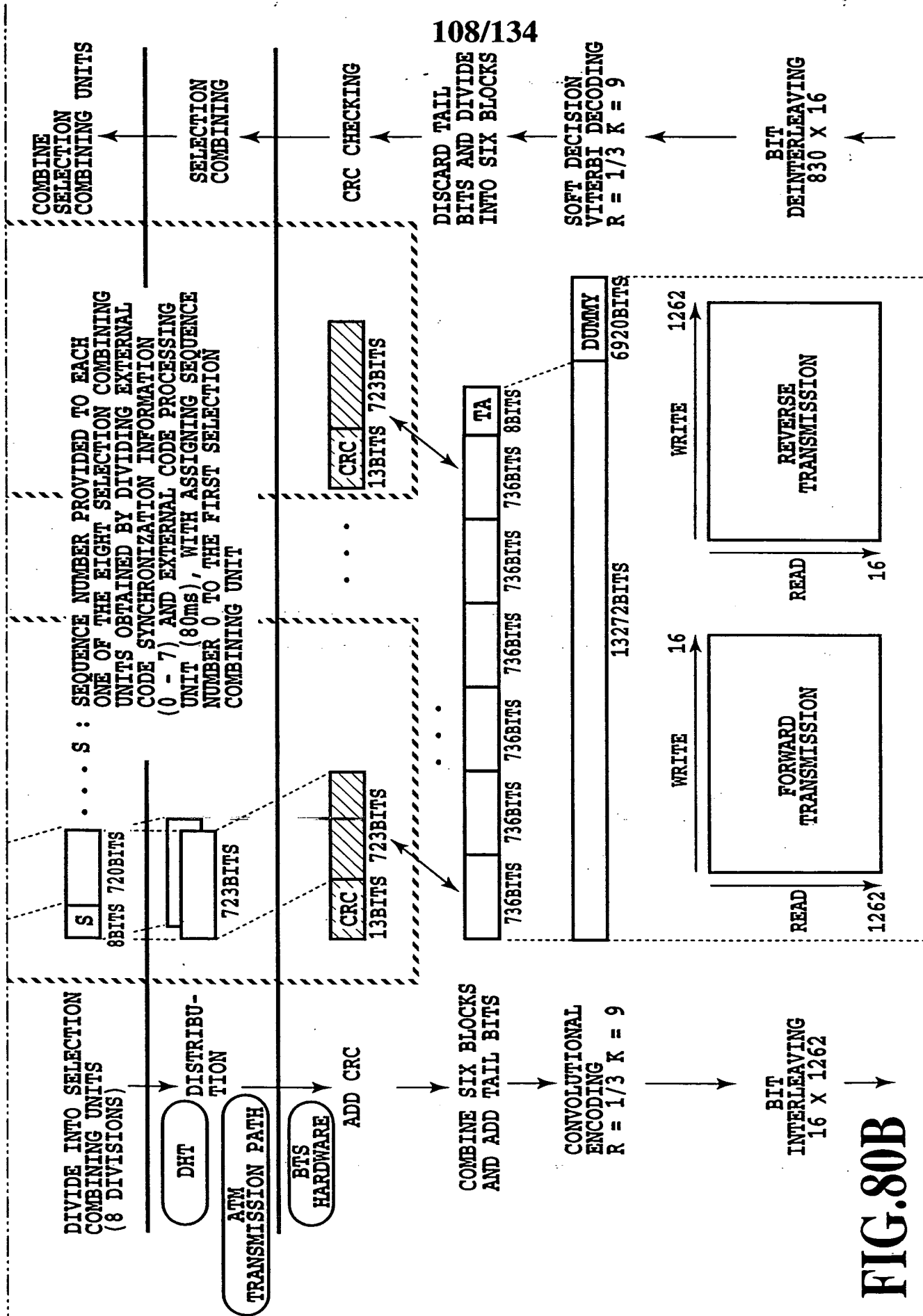


FIG.80A

6B = 384kbps





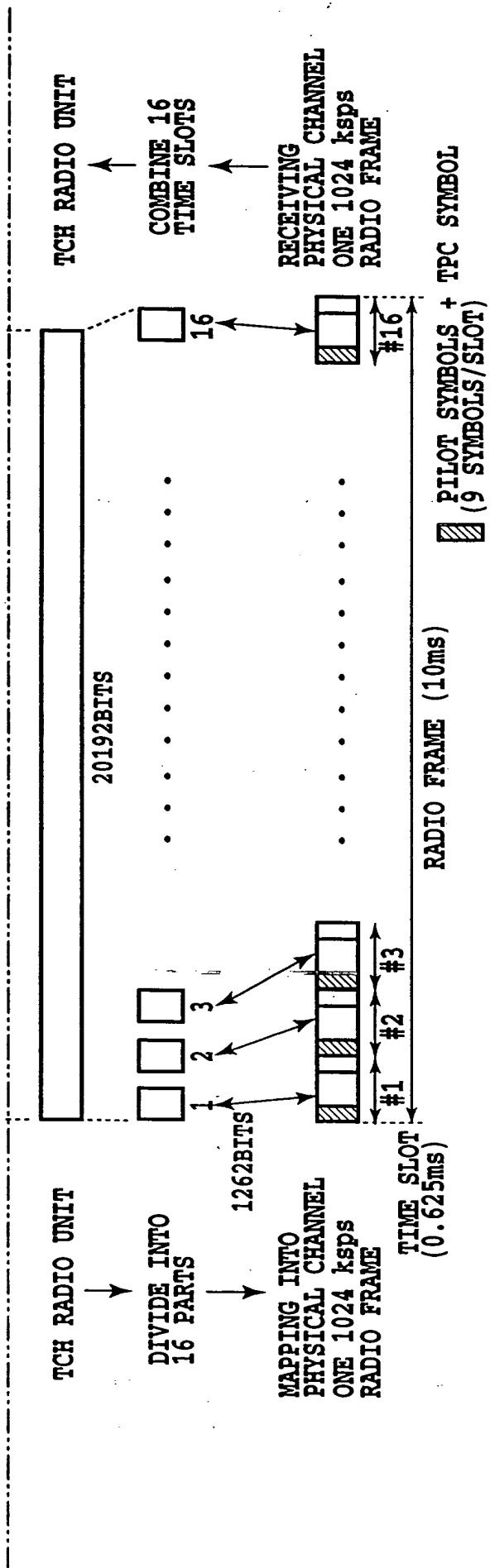


FIG.80C

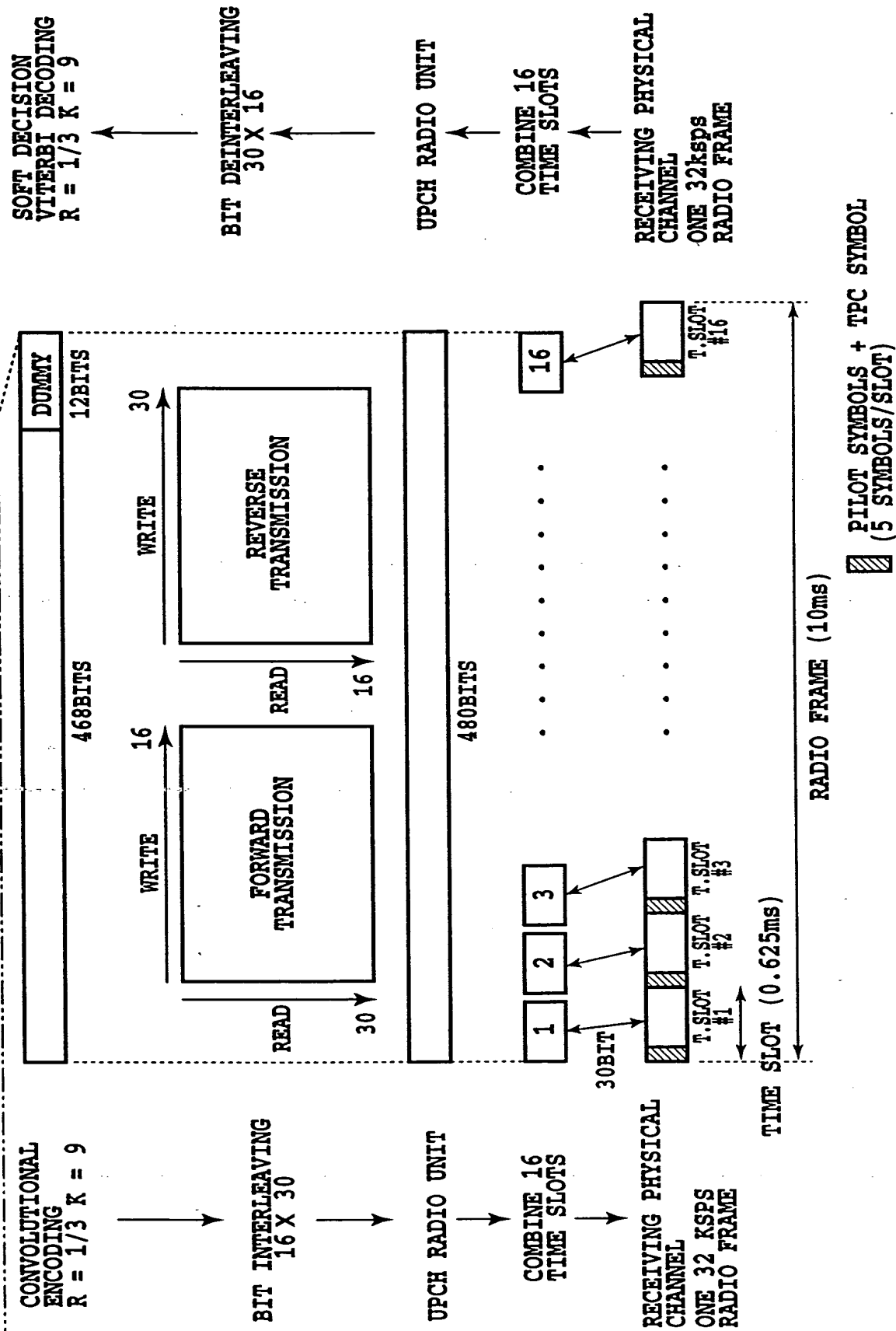


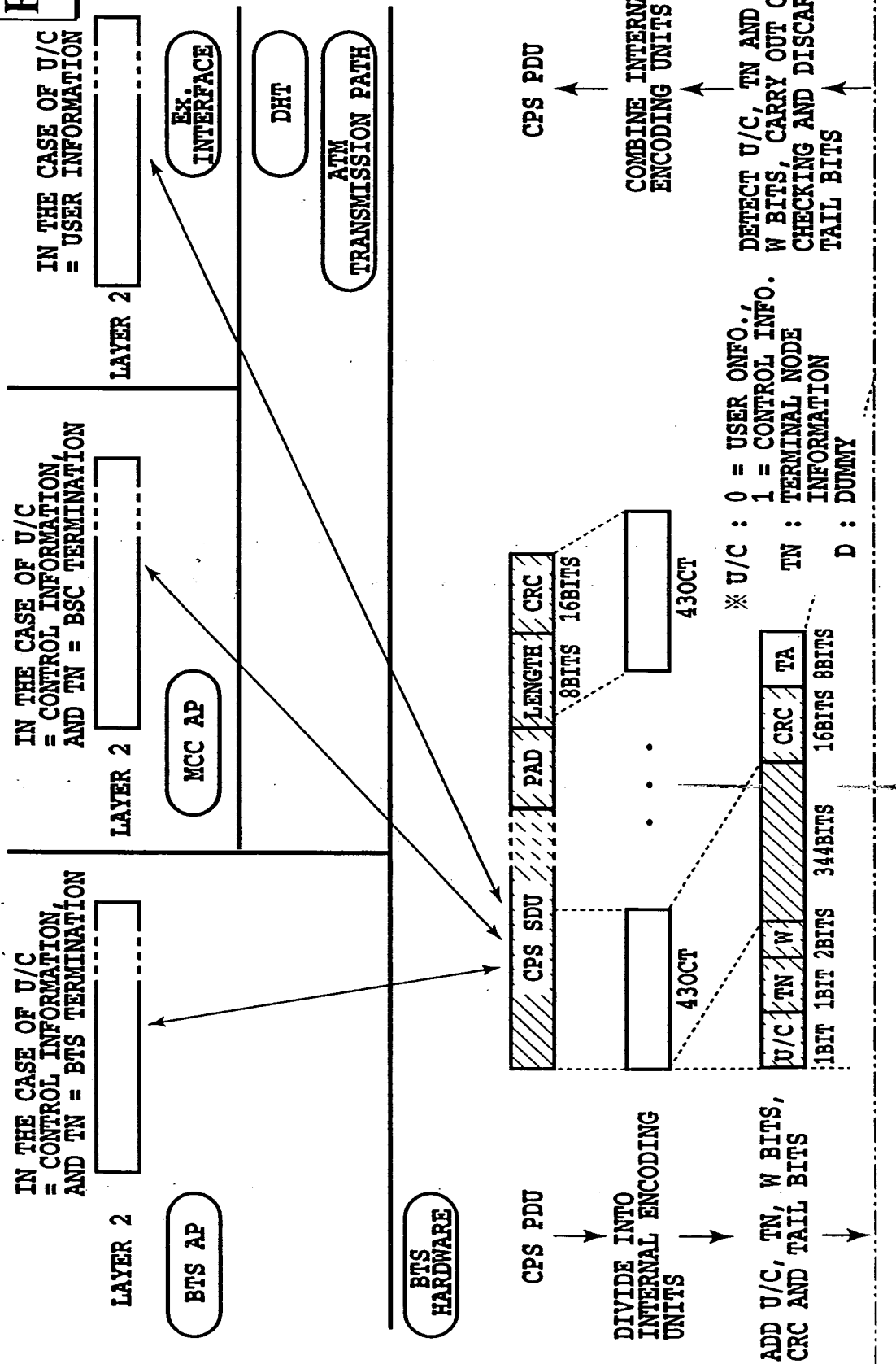
FIG.81B

FIG.82

FIG.82A

FIG.82B

FIG.82A



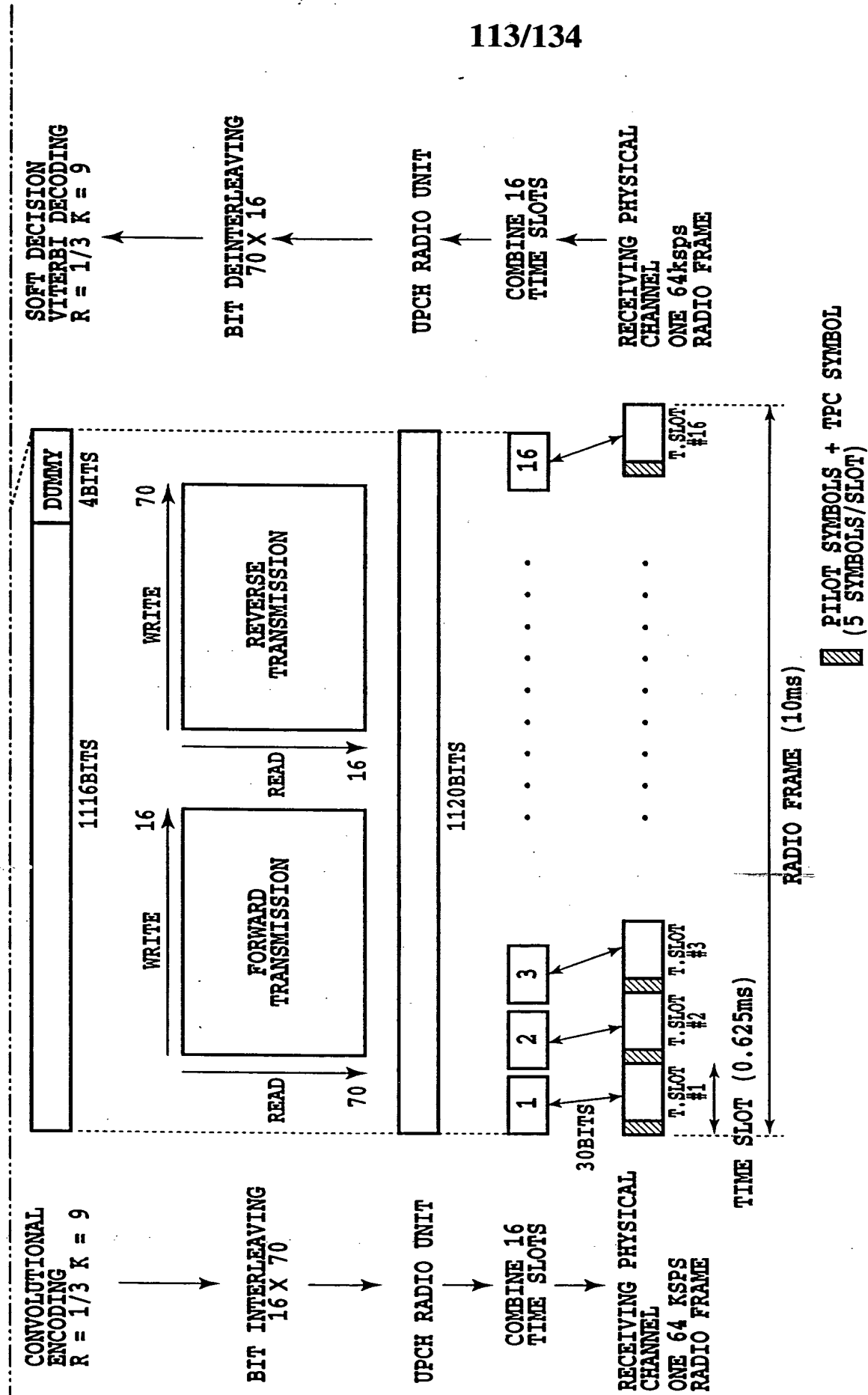


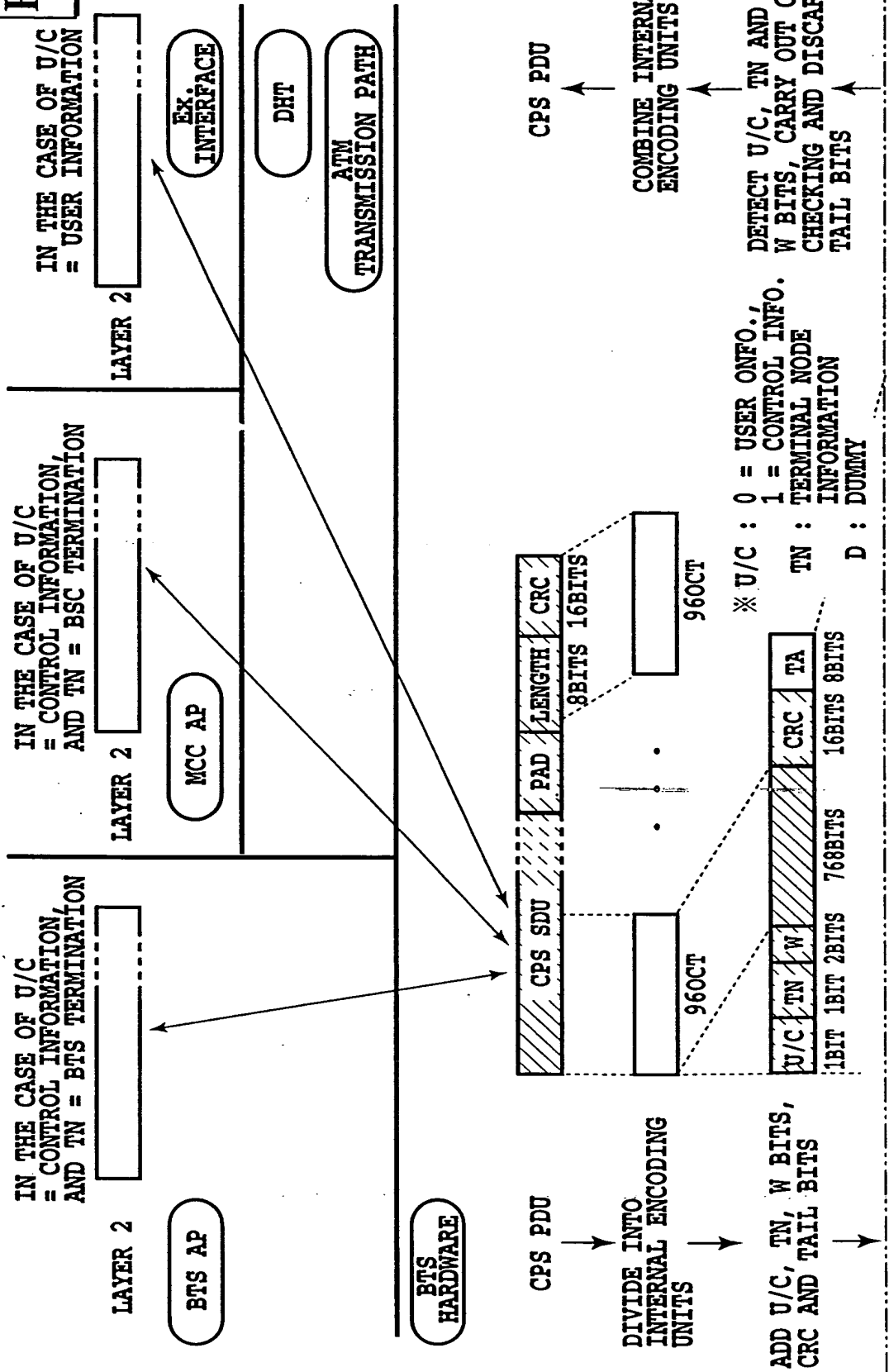
FIG.82B

FIG.83

FIG.83A

FIG.83B

FIG.83A



**CONVOLUTIONAL
ENCODING
R = 1/3 K = 9**

BIT DEINTERLEAVING
150 X 16

BIT INTERLEAVING
16 X 150

UPCH RADIO UNIT

UPCH RADIO UNIT

**COMBINE 16
TIME SLOTS**

**COMBINE 16
TIME SLOTS**

RECEIVING PHYSICAL
CHANNEL
ONE 128kps
RADIO FRAME

RECEIVING PHYSICAL
CHANNEL
ONE 128KSPS
RADIO FRAME

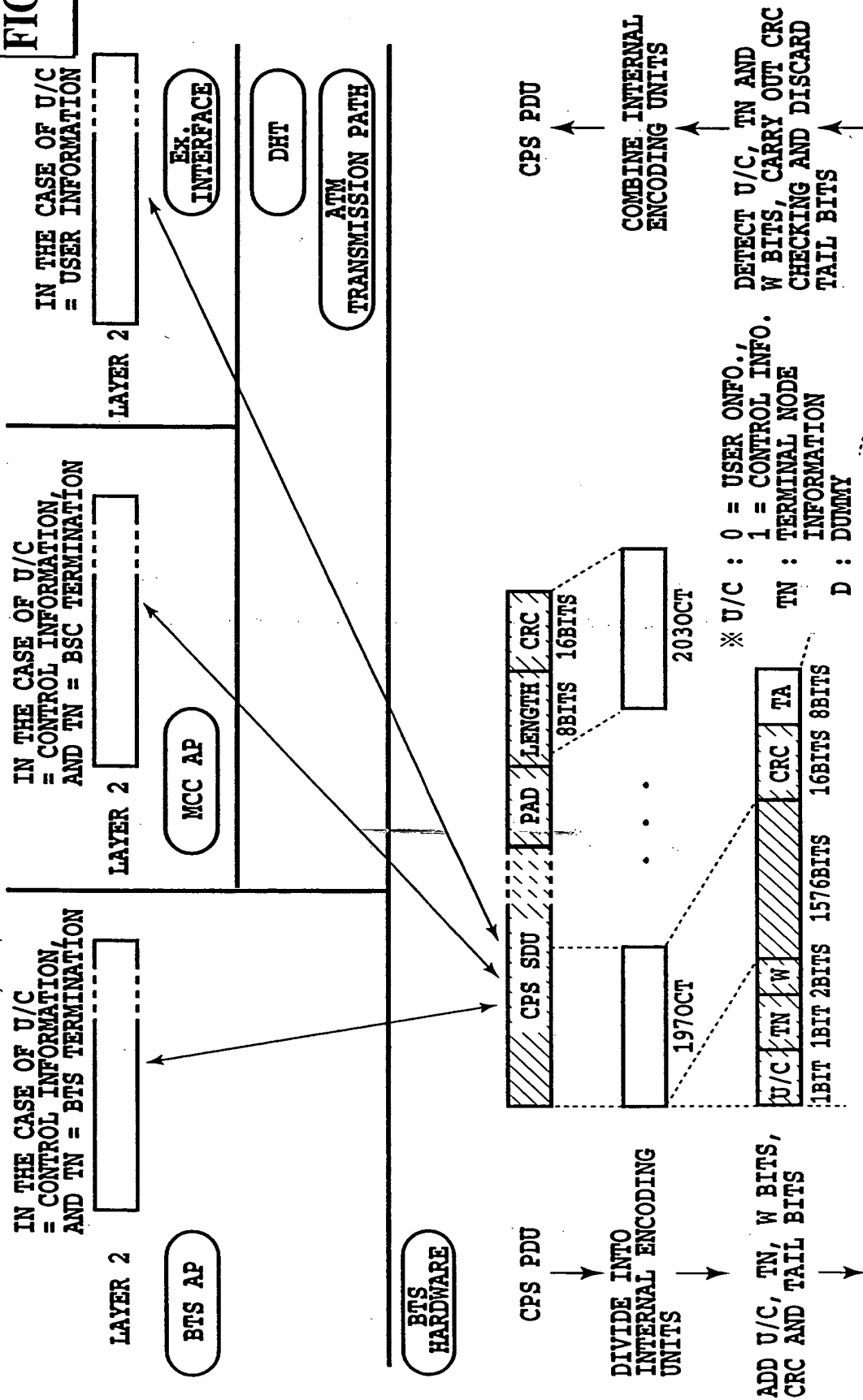


FIG.84

FIG.84A

FIG.84B

FIG.84A



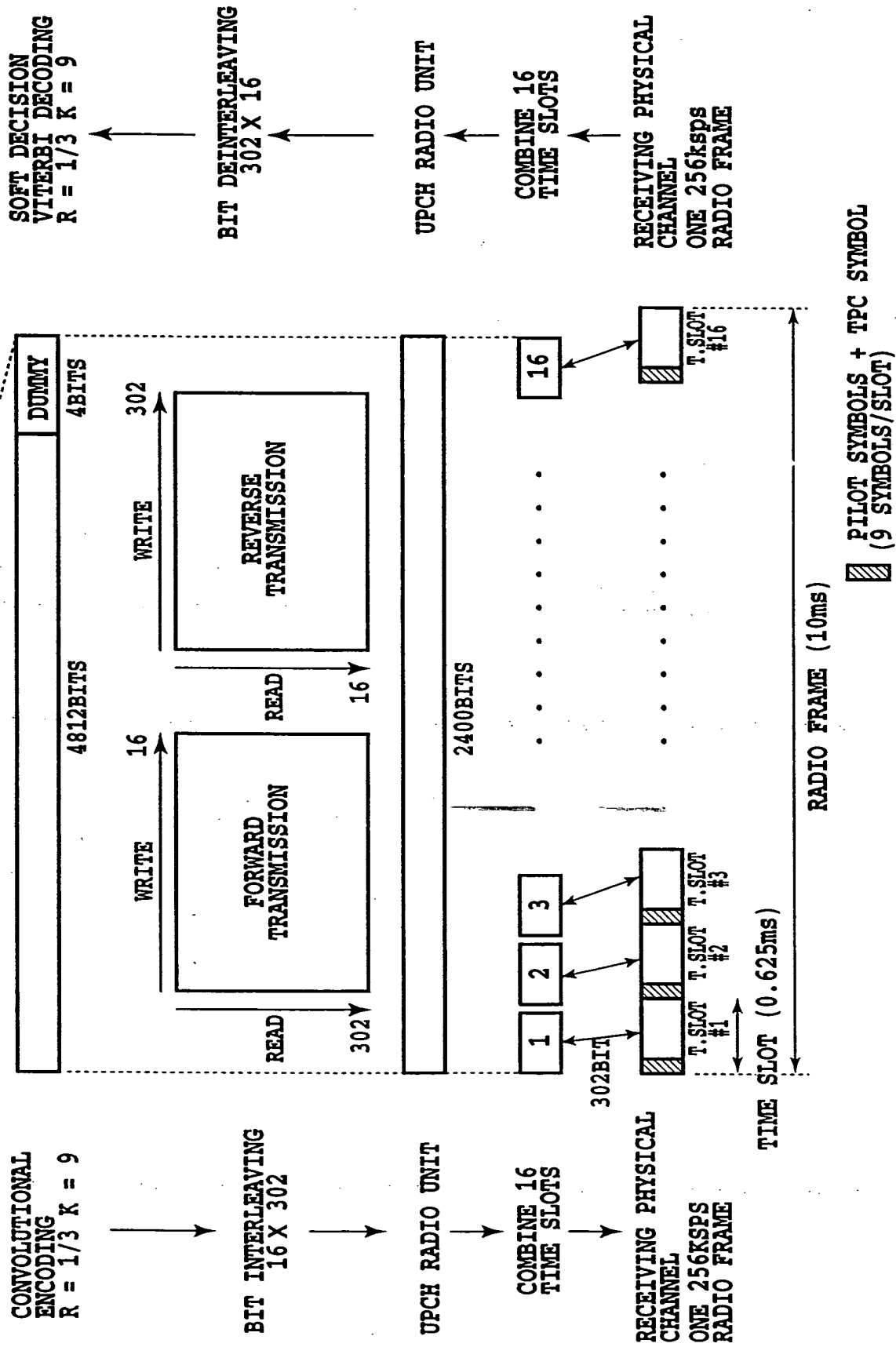


FIG.84B

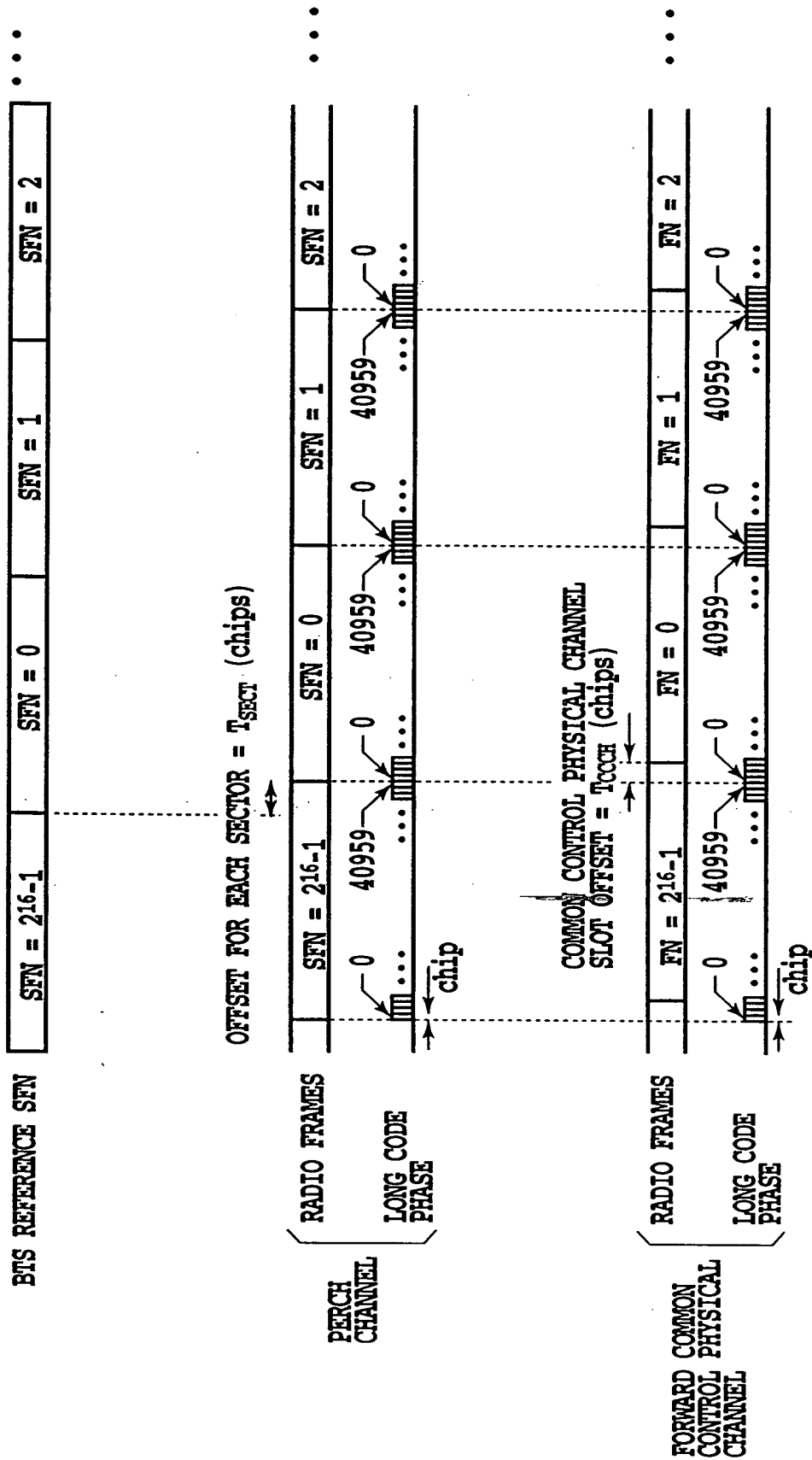


FIG.85

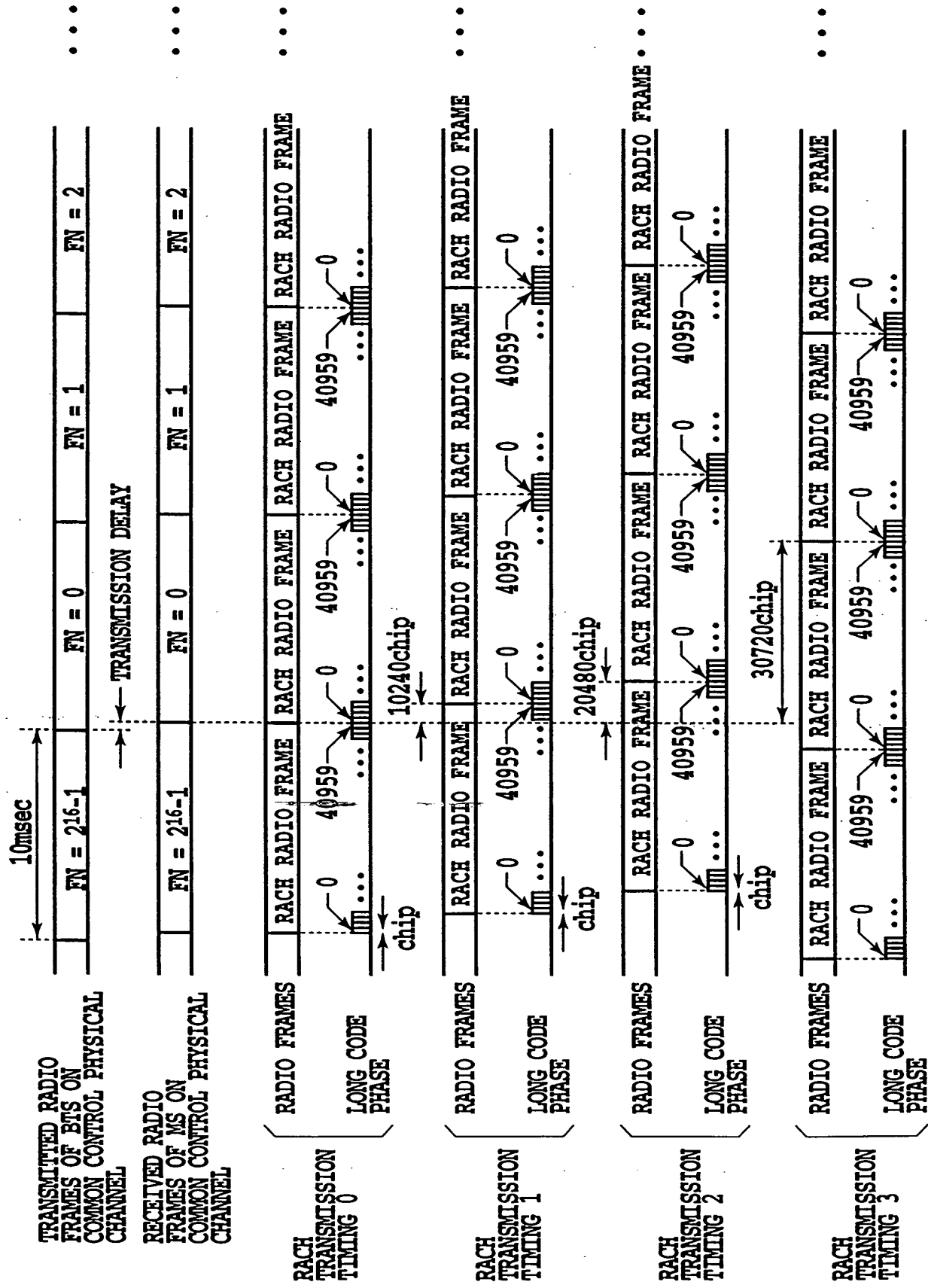


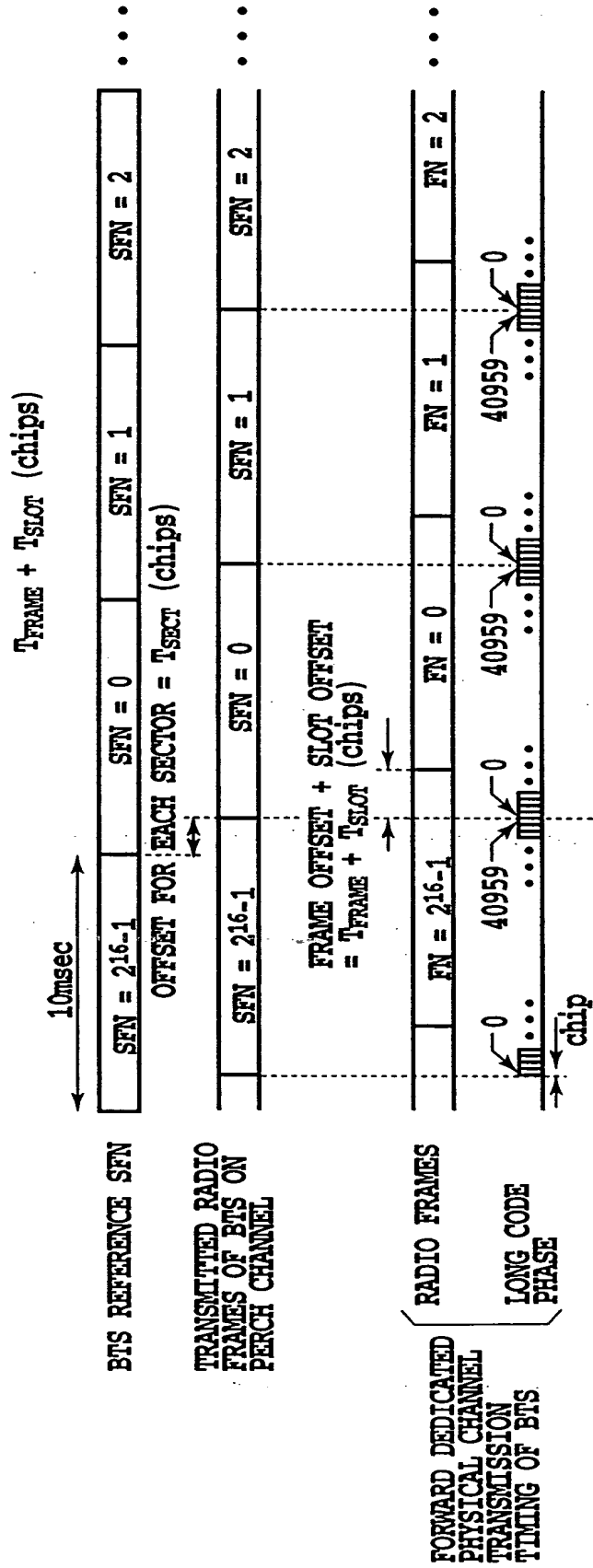
FIG.86

FIG.87

FIG.87A

FIG.87B

FIG.87A



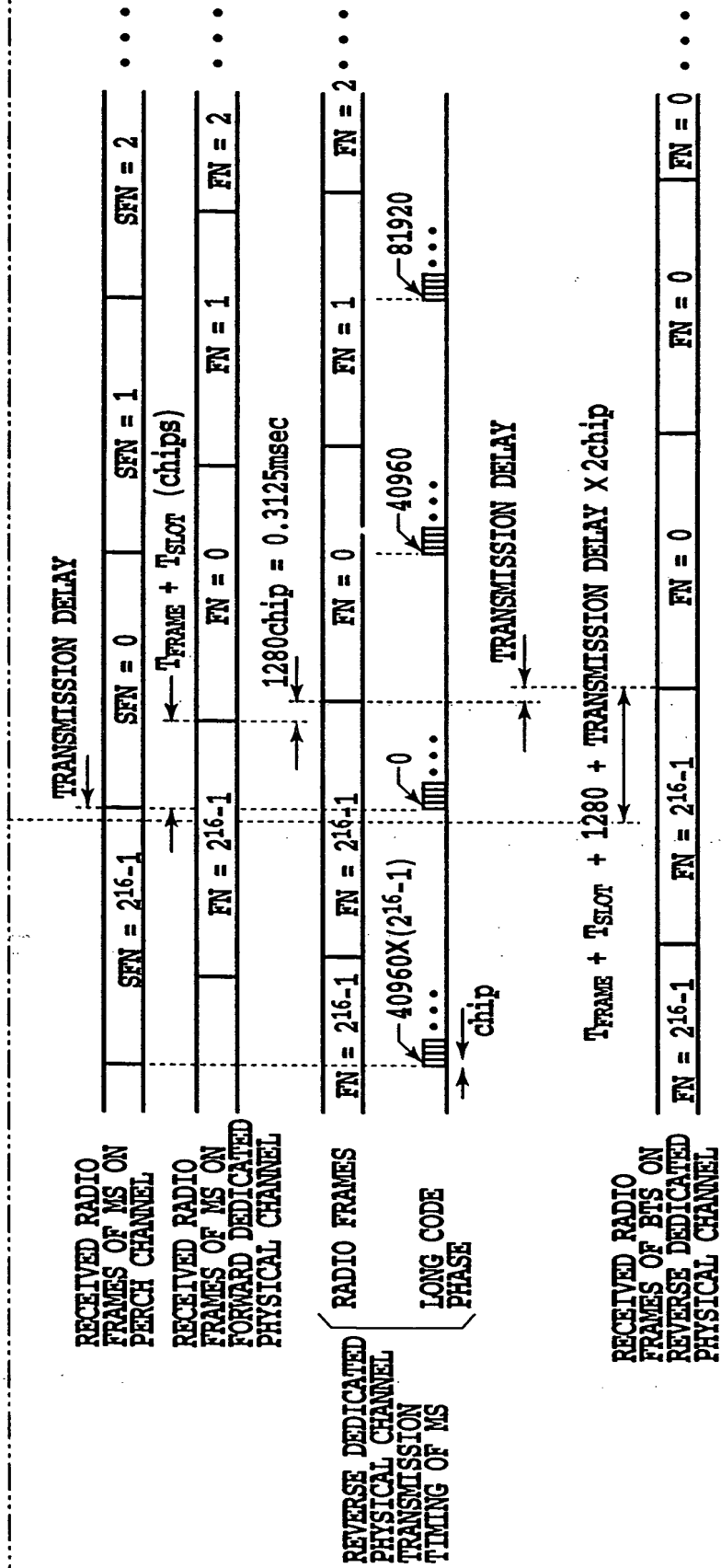


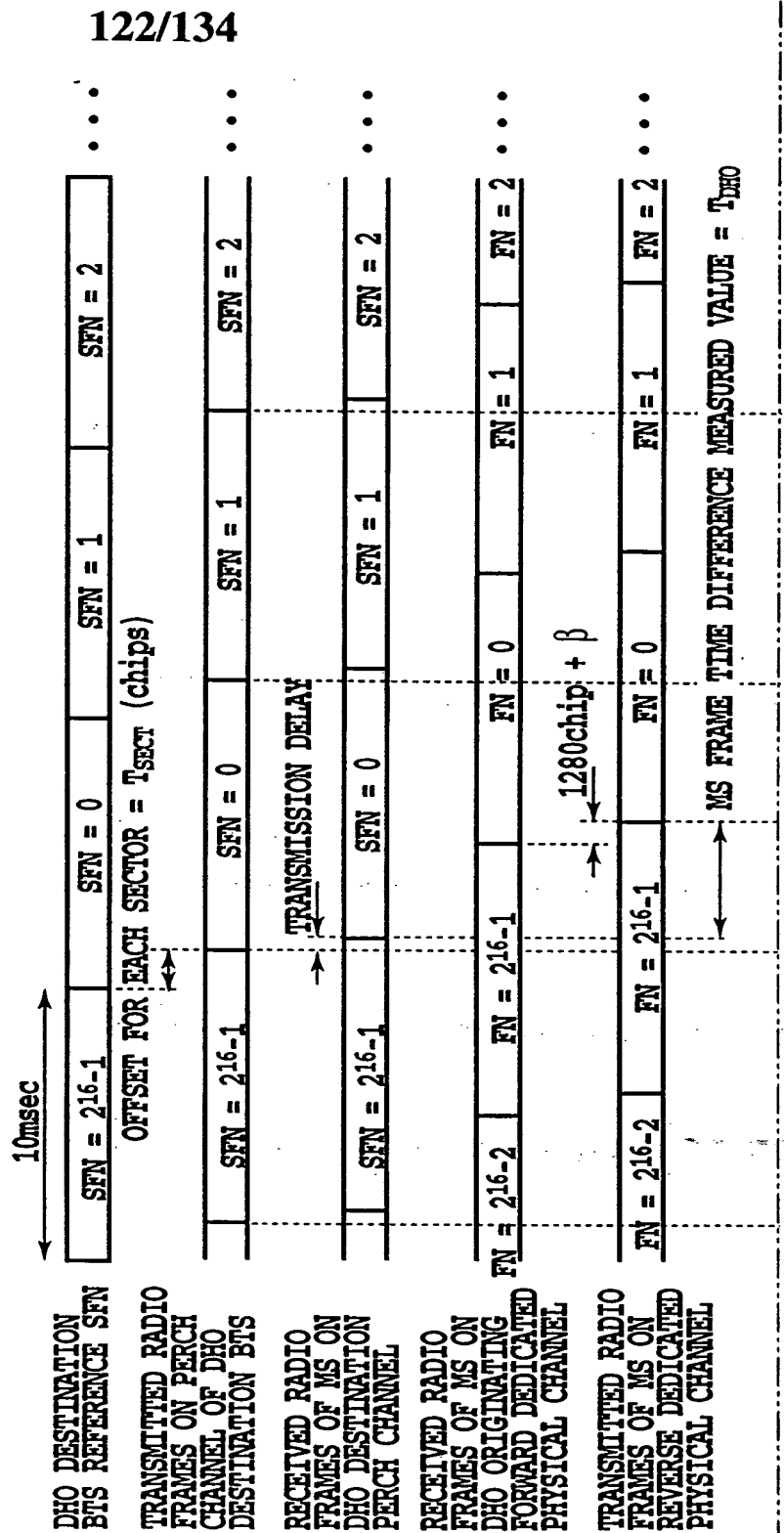
FIG.87B

FIG.88

FIG.88A

FIG.88B

FIG.88A



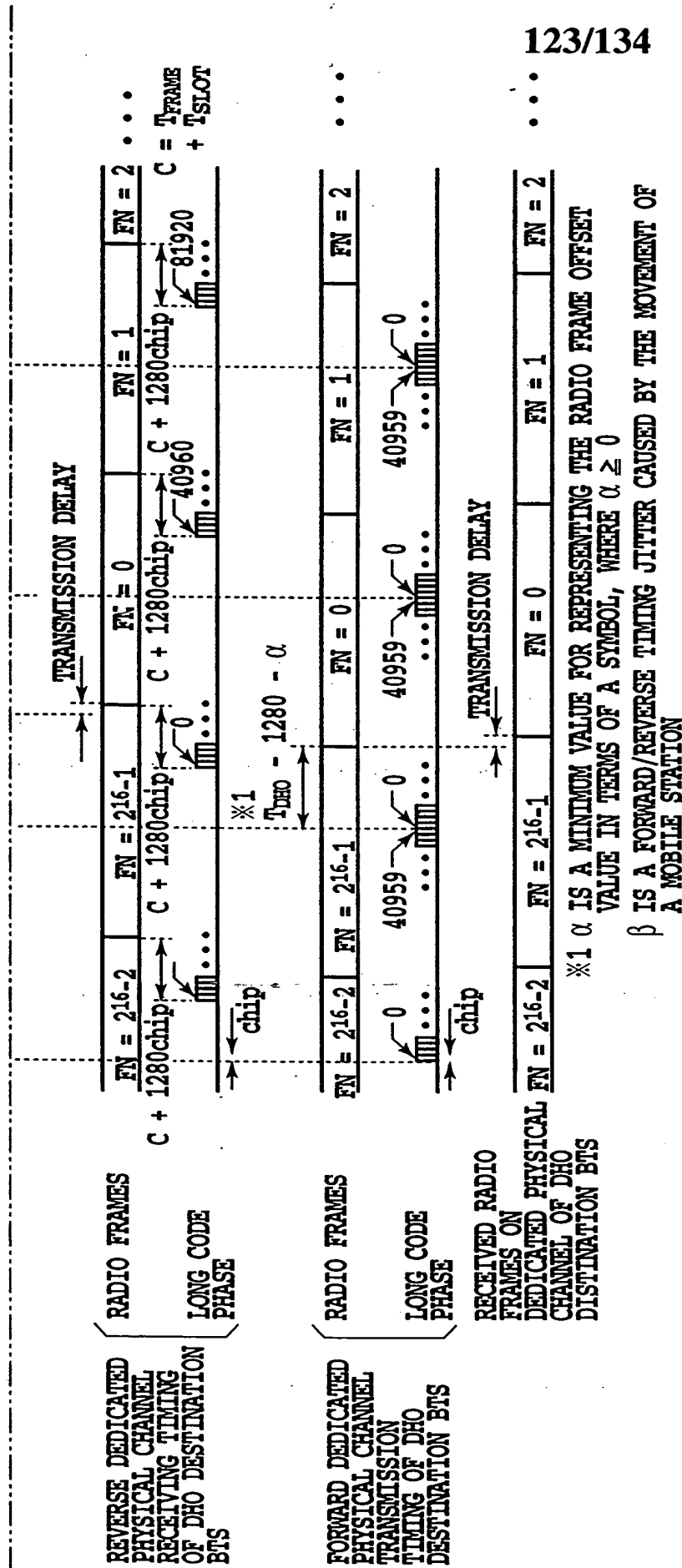


FIG.88B

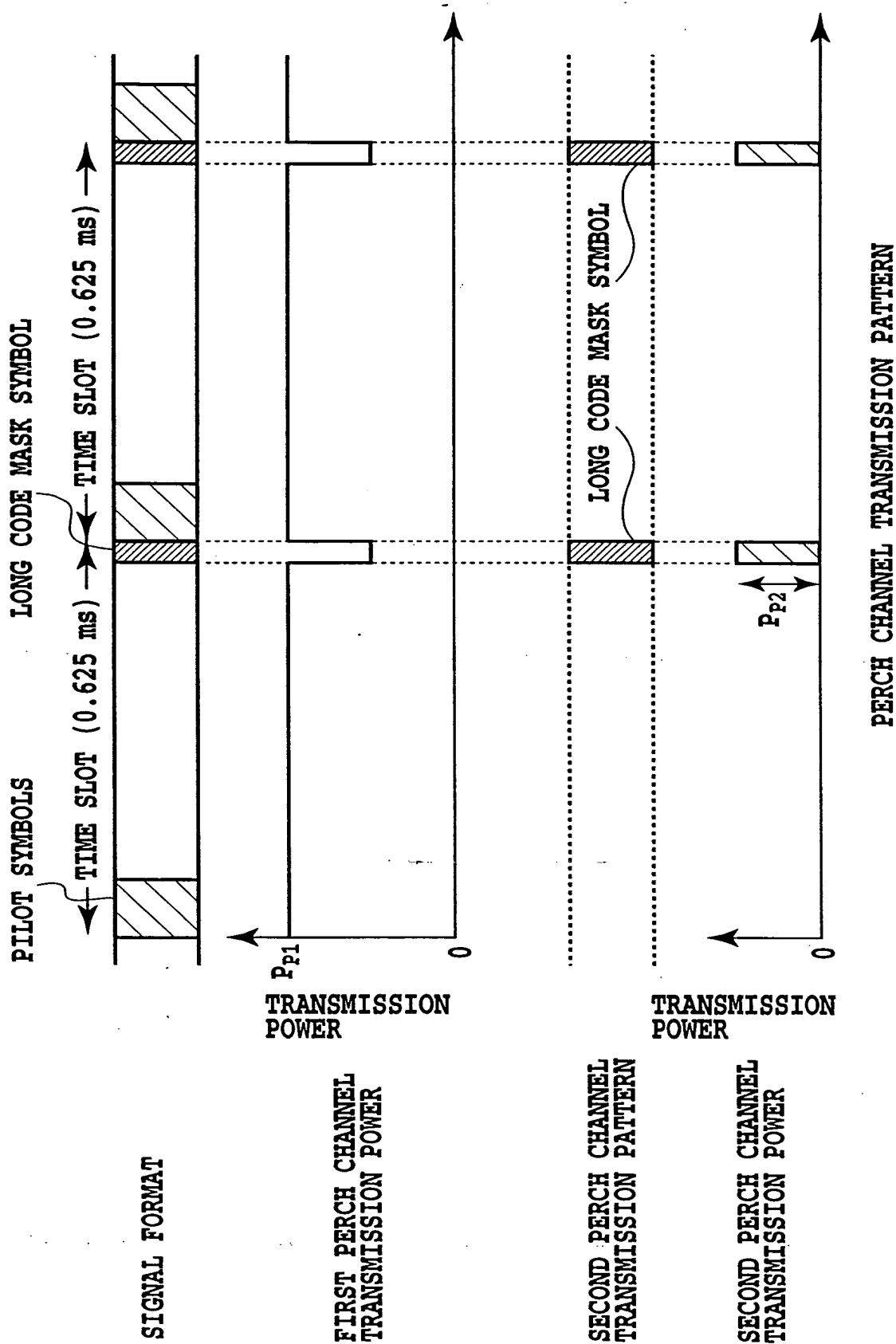


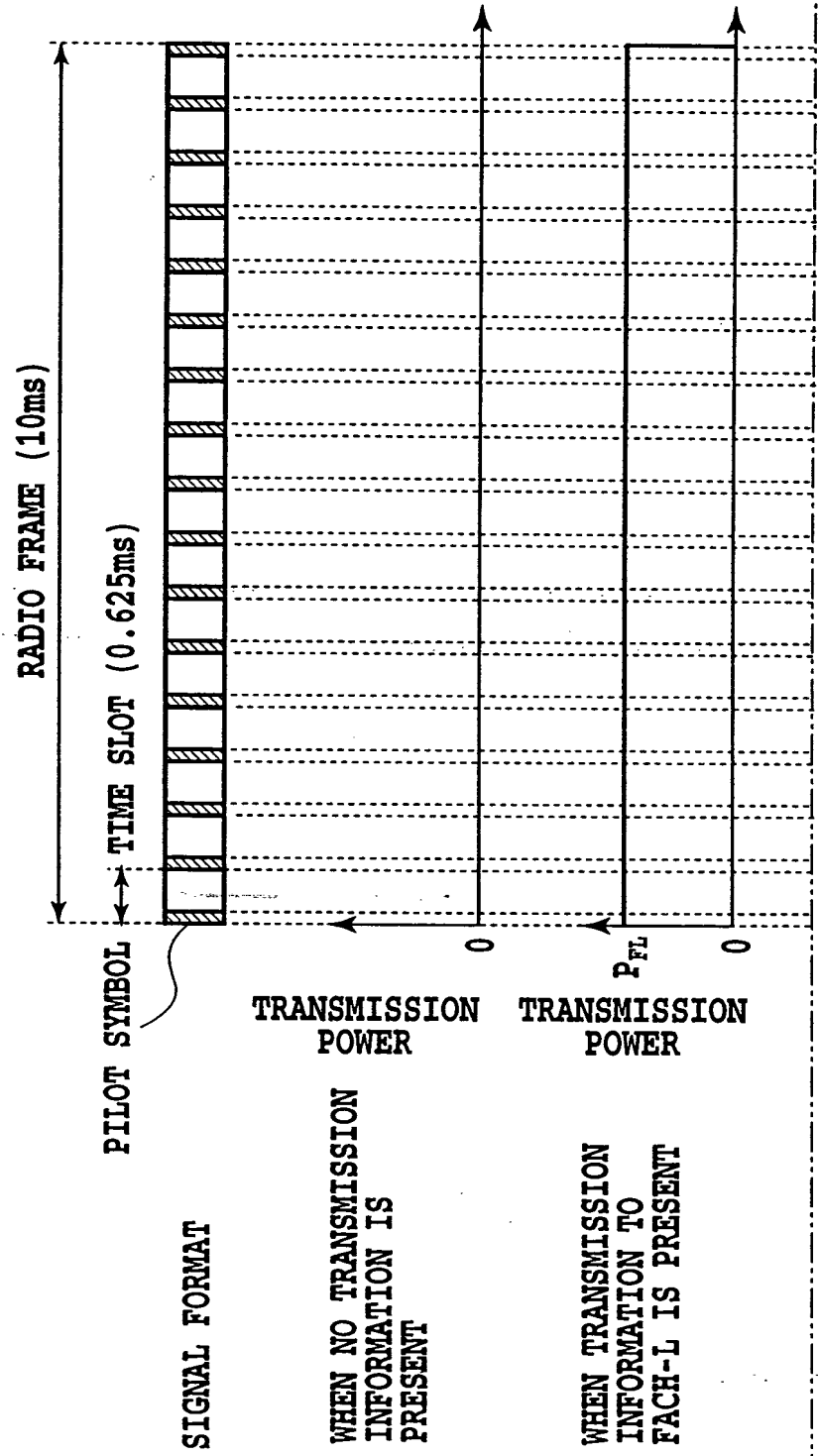
FIG.89

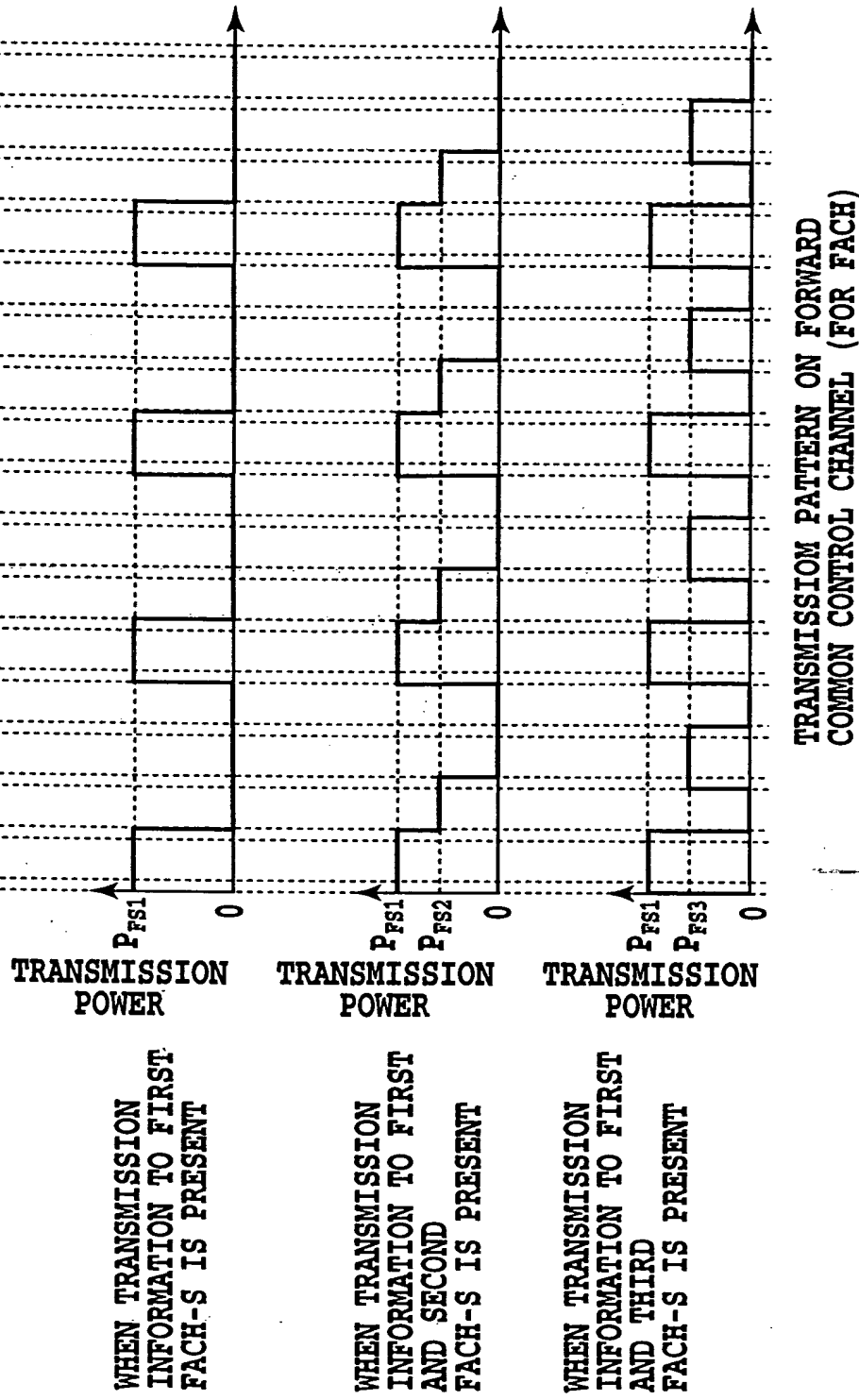
FIG.90

FIG.90A

FIG.90B

FIG.90A





TRANSMISSION PATTERN ON FORWARD
COMMON CONTROL CHANNEL (FOR FACH)

FIG.90B

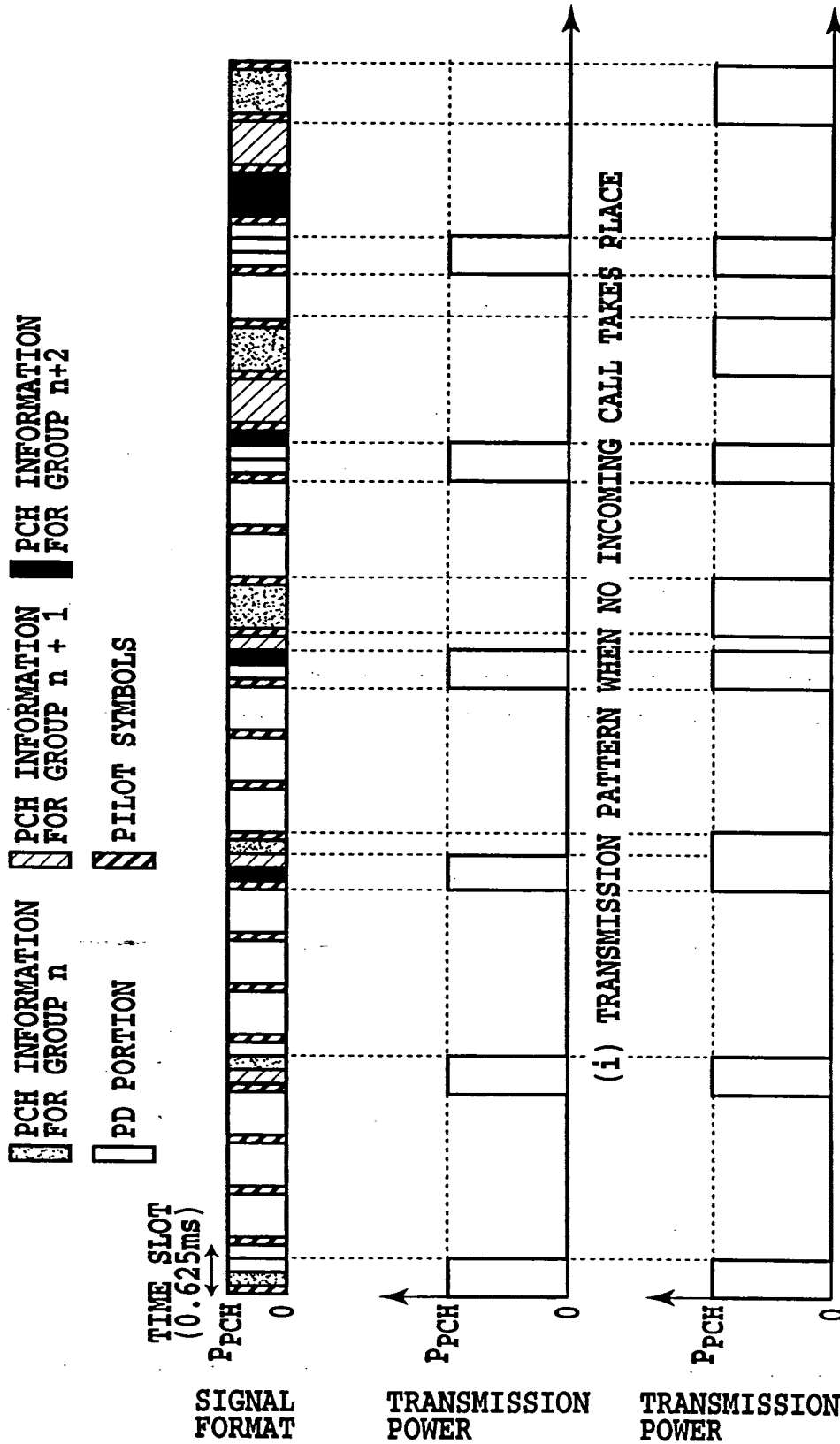
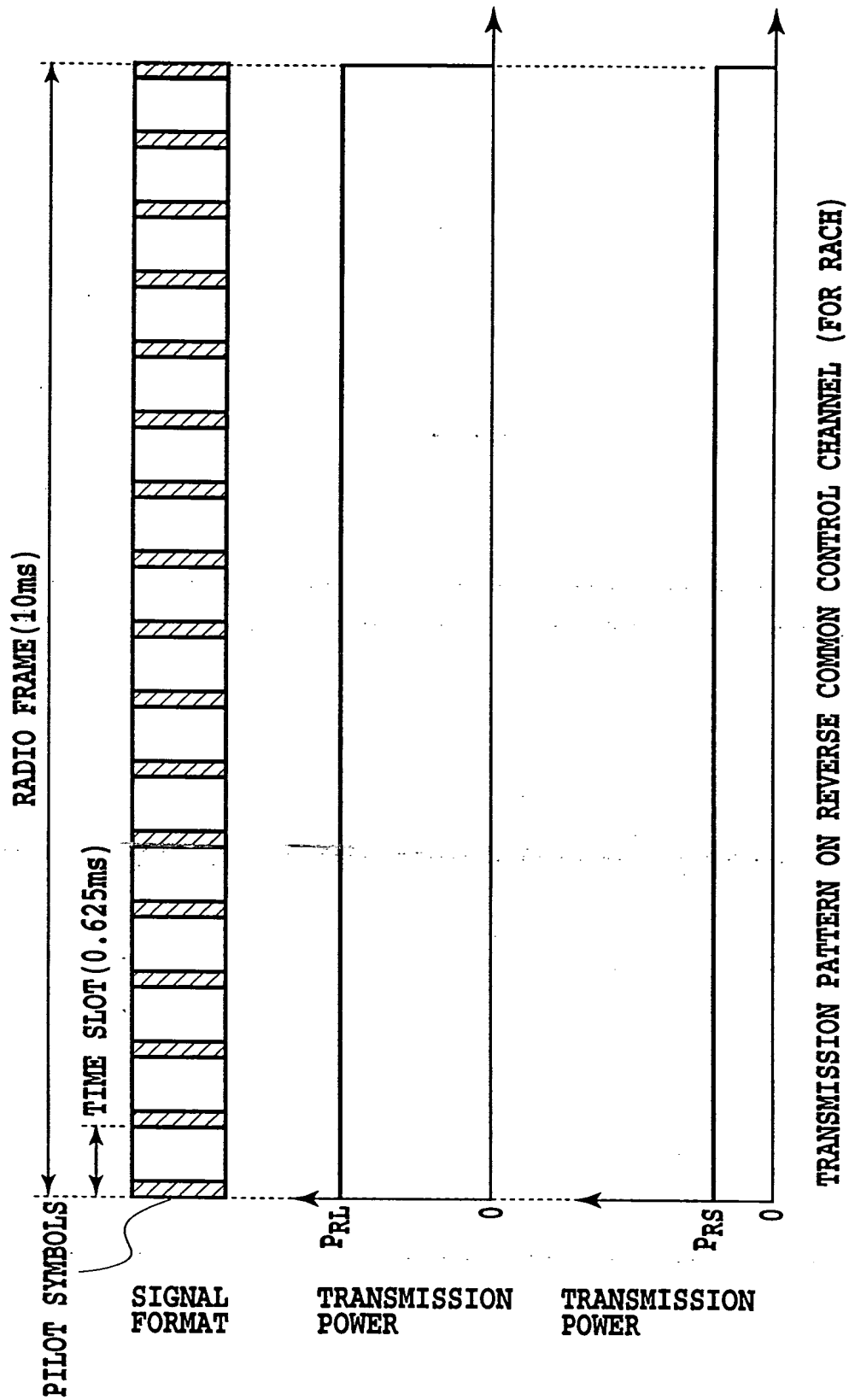


FIG.91

**FIG.92**

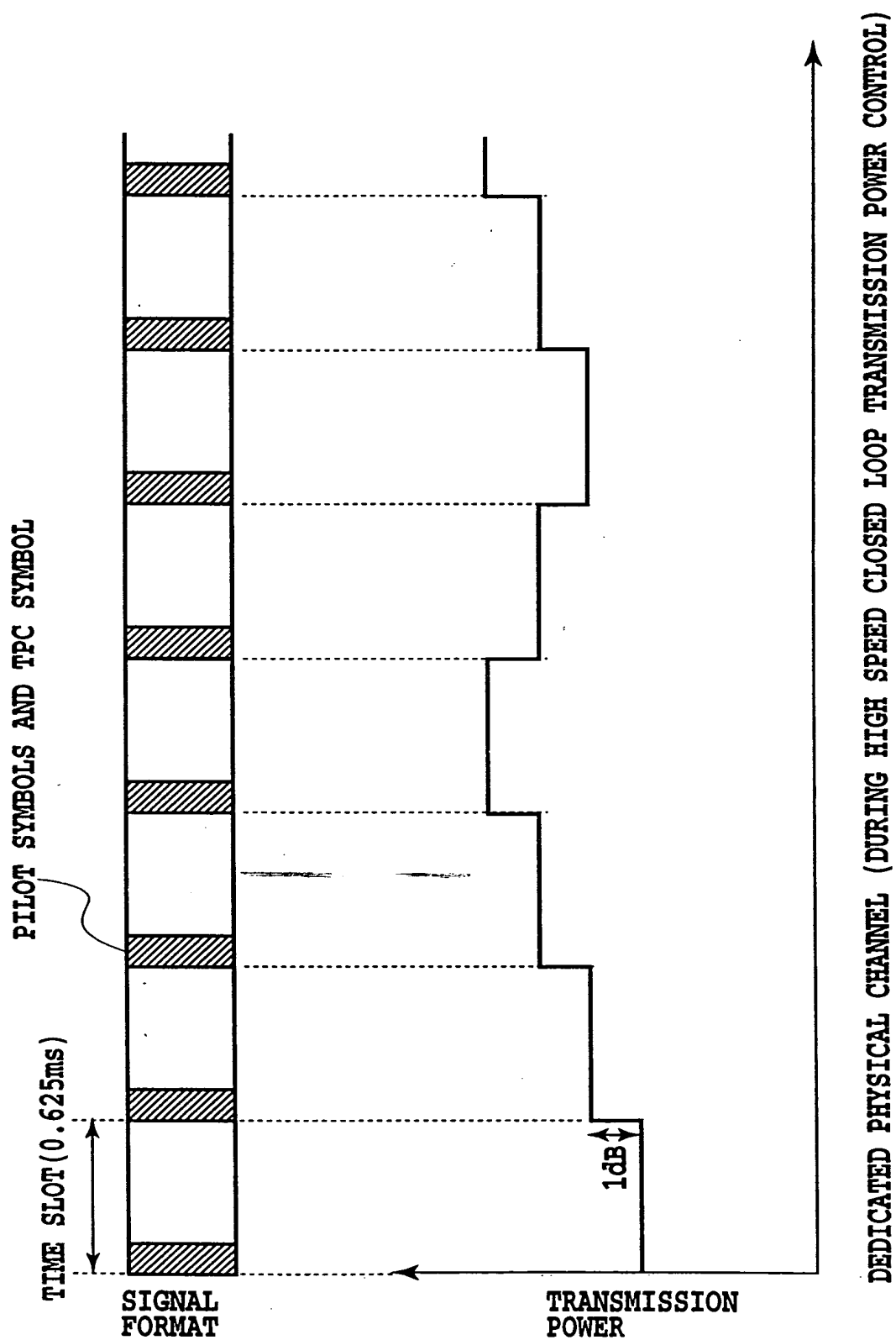
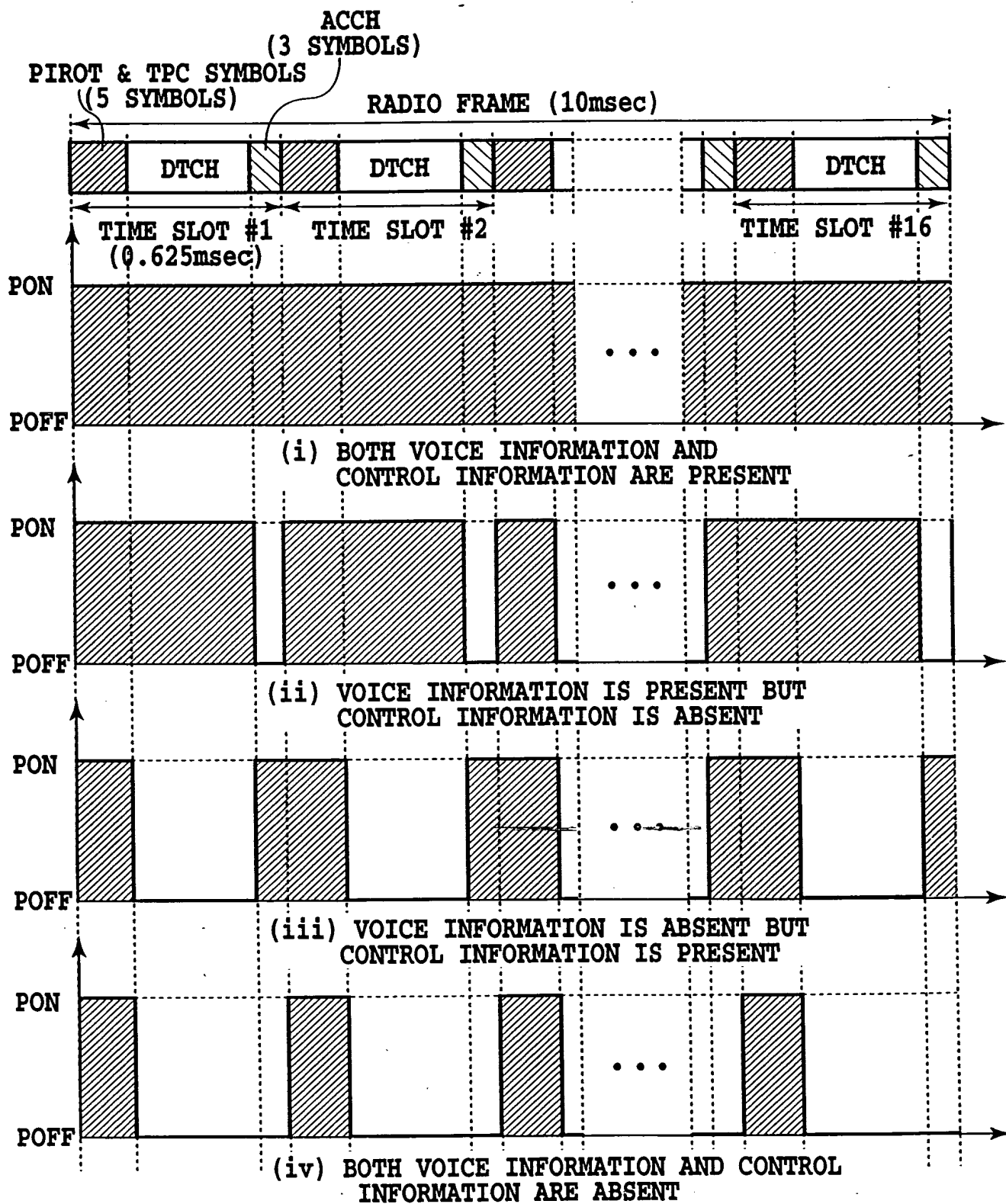


FIG.93



32 KSPS DEDICATED PHYSICAL CHANNEL (DTX CONTROL)

FIG.94

FIG.95

FIG.95A

FIG.95B

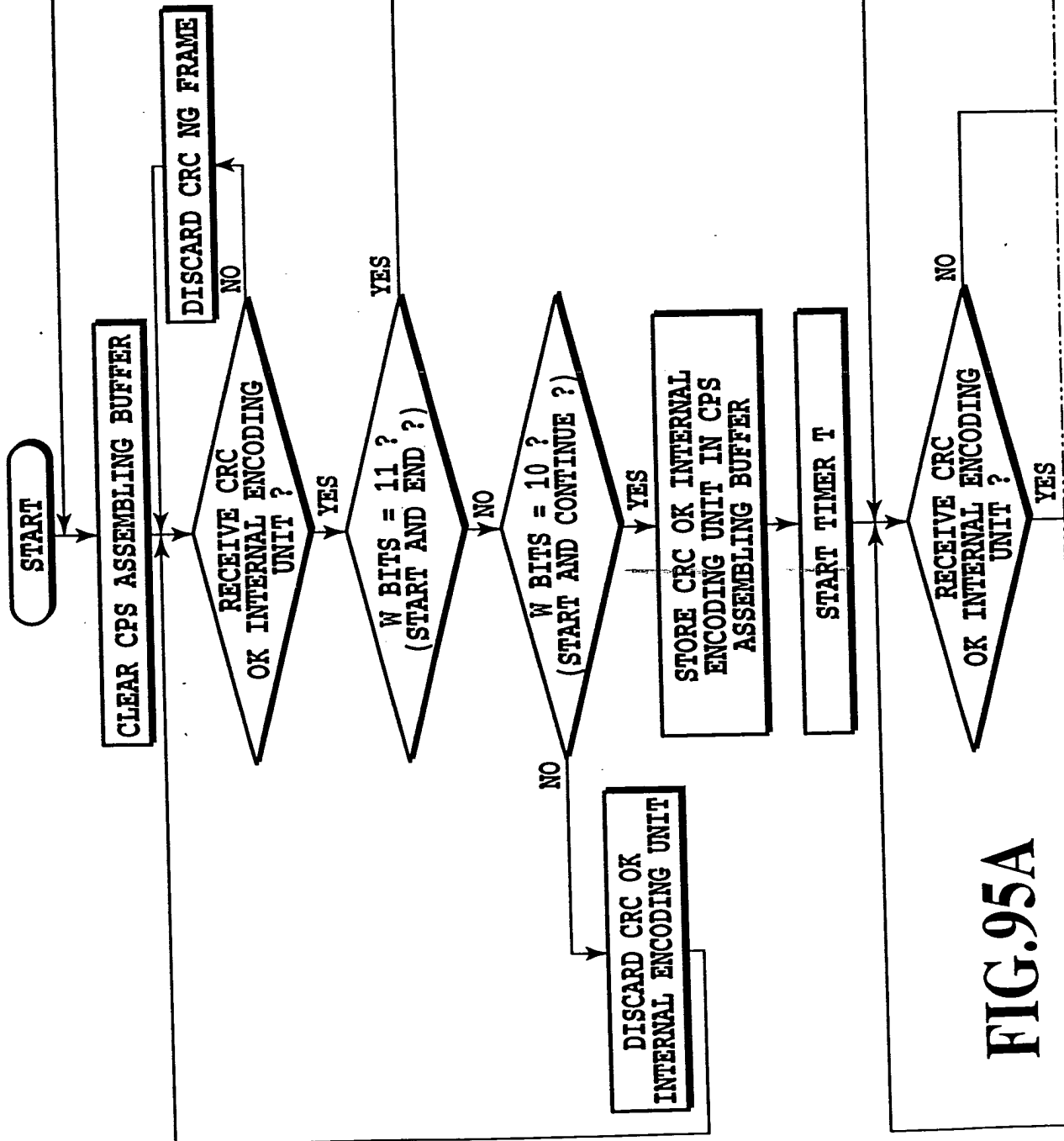


FIG.95A

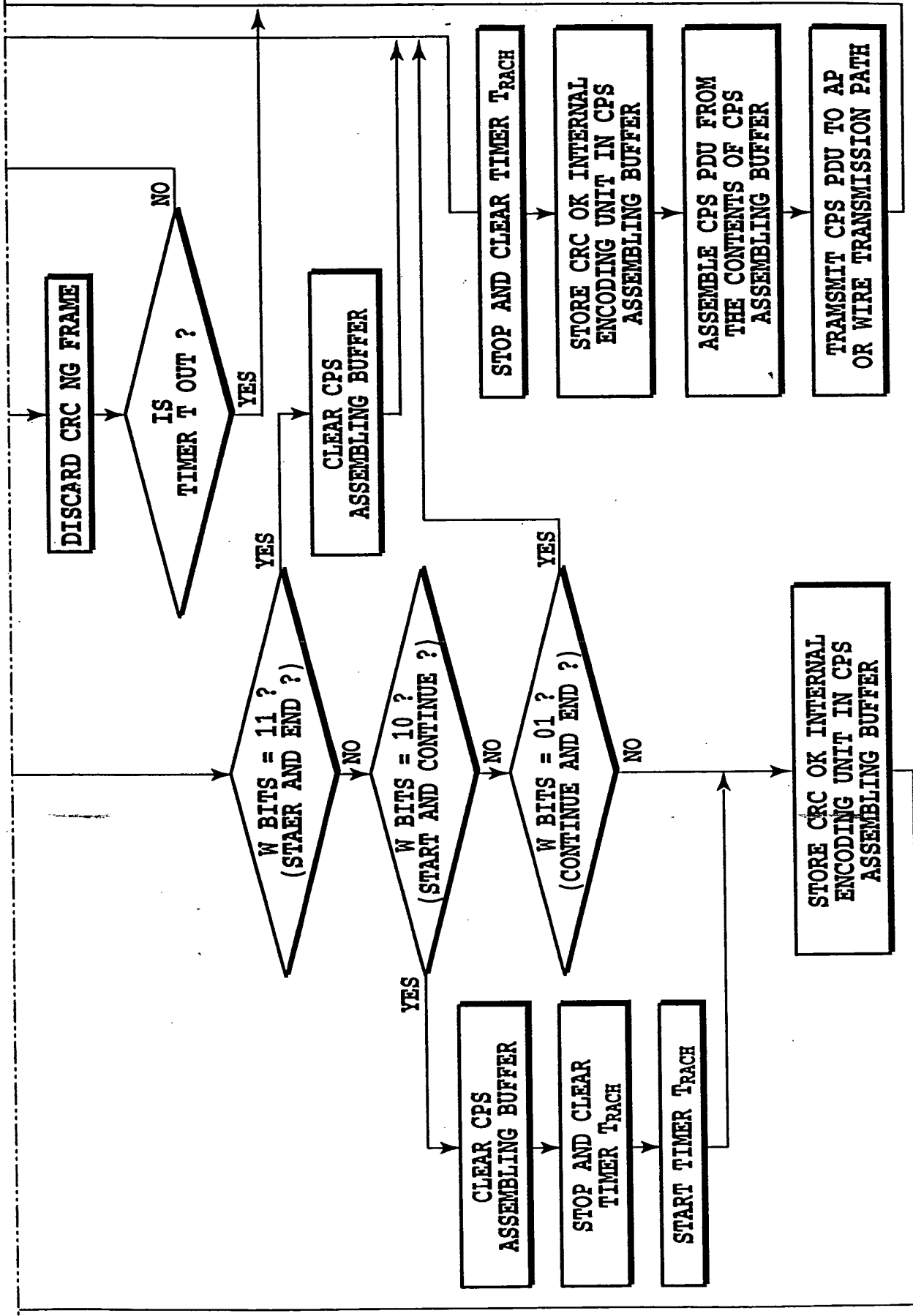


FIG.95B

FIG.96

FIG.96A

FIG.96B

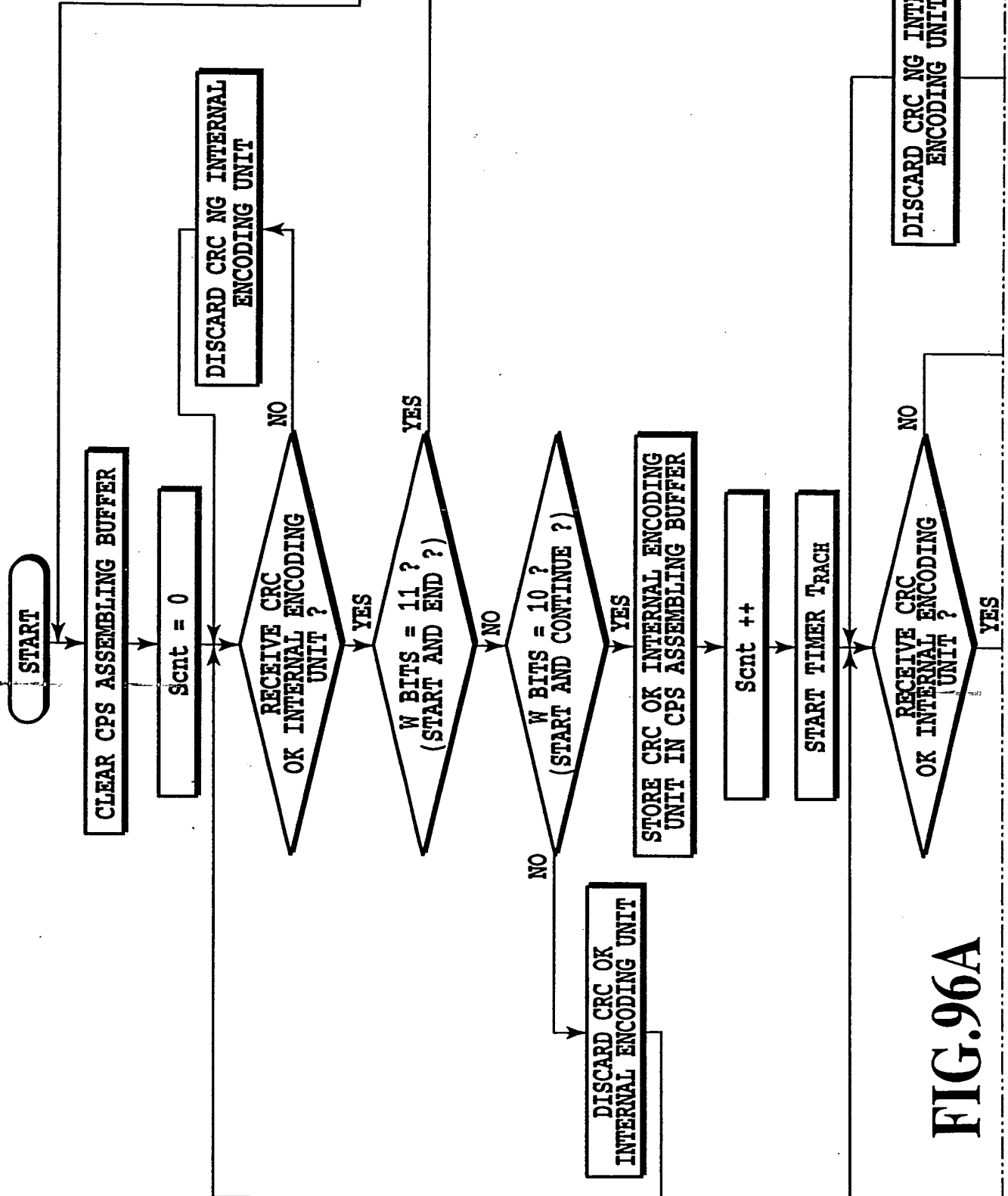


FIG.96A

FIG. 96B